

Compal Confidential

Model Name : P3MJ0  
File Name : LA-7121P  
BOM P/N:43XXXXXXL01(UMA)  
43XXXXXXL02(DIS)

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M/B Schematics Document

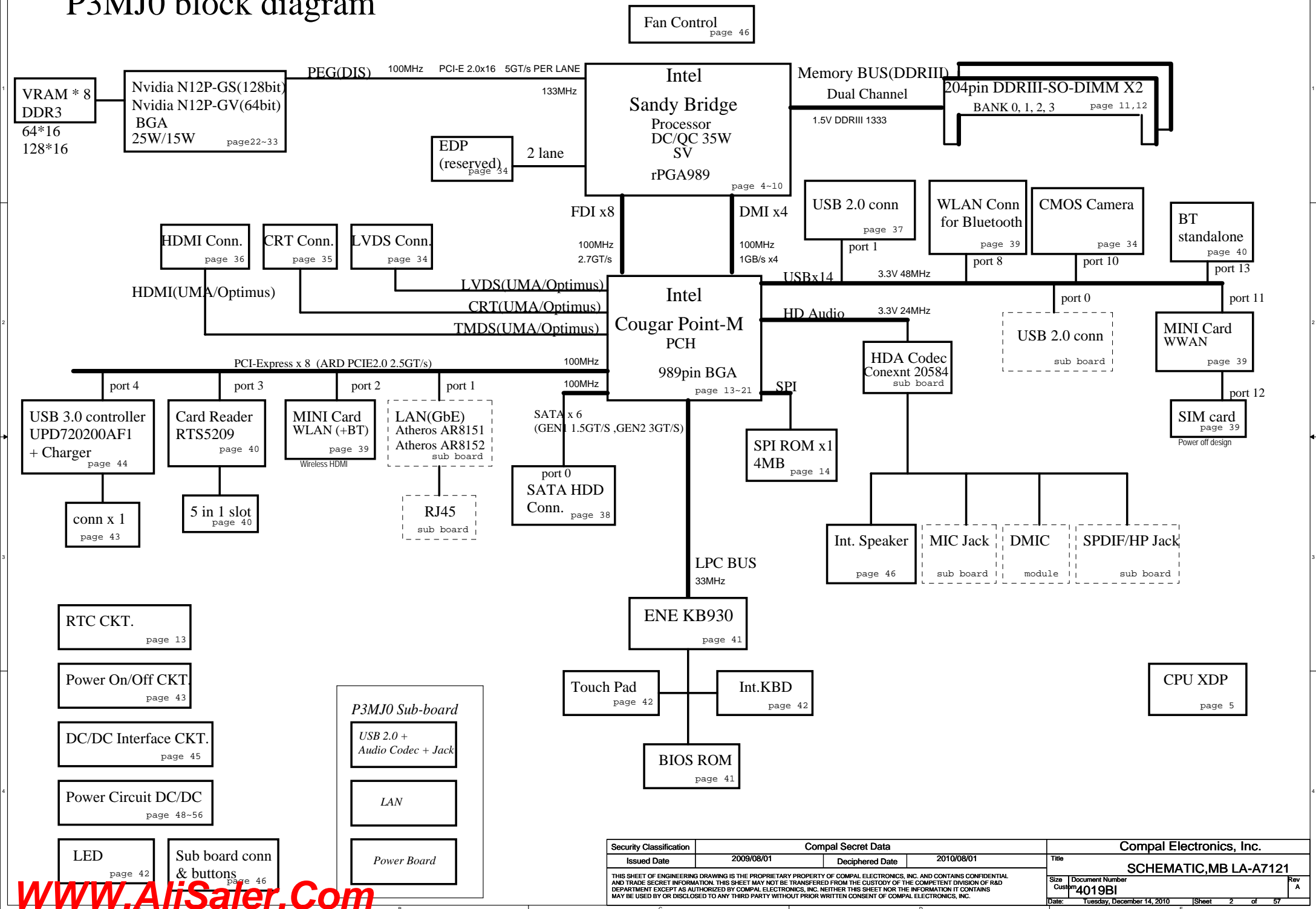
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH  
Nvidia N12P-GS/GV

2010-11-16

REV:0.2

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# P3MJ0 block diagram



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT Config

3G SKU: 3G@  
BT SKU: BT@

BOM Config

UMA Only: UMA@ /BT@/3G@  
N12P-GS OPTIMUS: OPT@/GS@/X76@/BT@/3G@  
N12P-GV OPTIMUS: OPT@/GV@/X76@/BT@/3G@

VRAM BOM Config  
add later

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMA@
Discrete(OPTIMUS)	OPT@
VRAM	X76@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
N12P-GS	GS@
N12P-GV	GV@

Project ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_PID min	VAD_PID typ	VAD_PID max
JM30	0	0 V	0 V	0 V
JM40	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
JM50	18K +/- 5%	0.436 V	0.503 V	0.538 V
SJM30	33K +/- 5%	0.712 V	0.819 V	0.875 V
SJM40	56K +/- 5%	1.036 V	1.185 V	1.264 V
SJM50	100K +/- 5%	1.453 V	1.650 V	1.759 V
NC	NC			
NC	NC			

USB Port Table

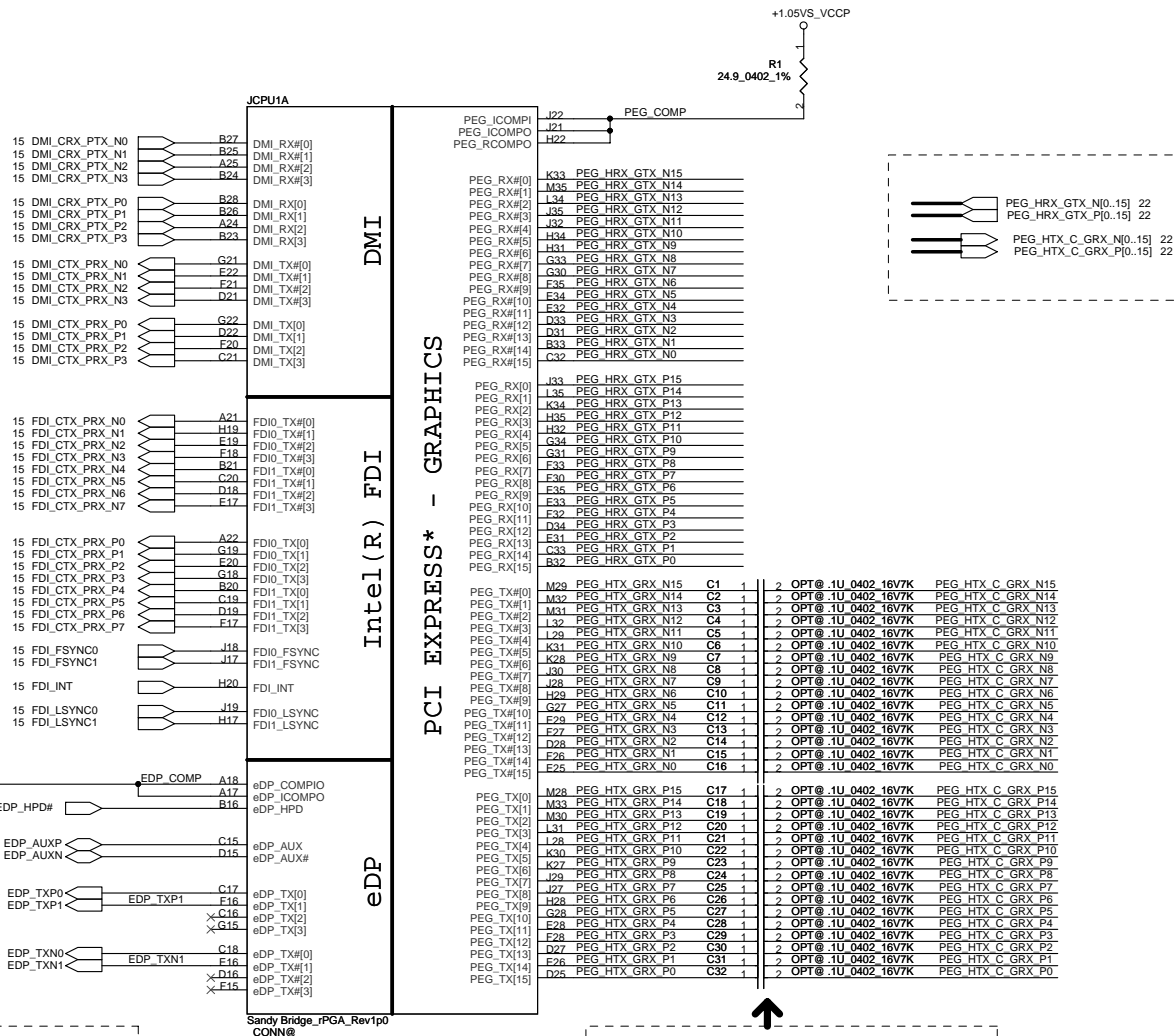
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Left Side)
		1	USB/B (Left Side)
	UHCI1	2	
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	Mini Card(WWAN)
	UHCI5	10	Camera
		11	
	UHCI6	12	SIM Card
		13	Blue Tooth

Design Common

schematics pages sequence	Part count location define
CPU/PCH/CLK	1~1099
DIMM	2000~2099
dGPU	1400~1999
LVDS/CRT/HDMI/DP	2100~2199
Audio	1100~1199
LAN	1200~1299
Card Reader	1300~1399
Other IO (HDD/ODD/MINI/USB/KBD/BIOS/ Button/LED)	2400~xxxx
KBC	2200~2299
POK CKT, DC/DC	2300~2399

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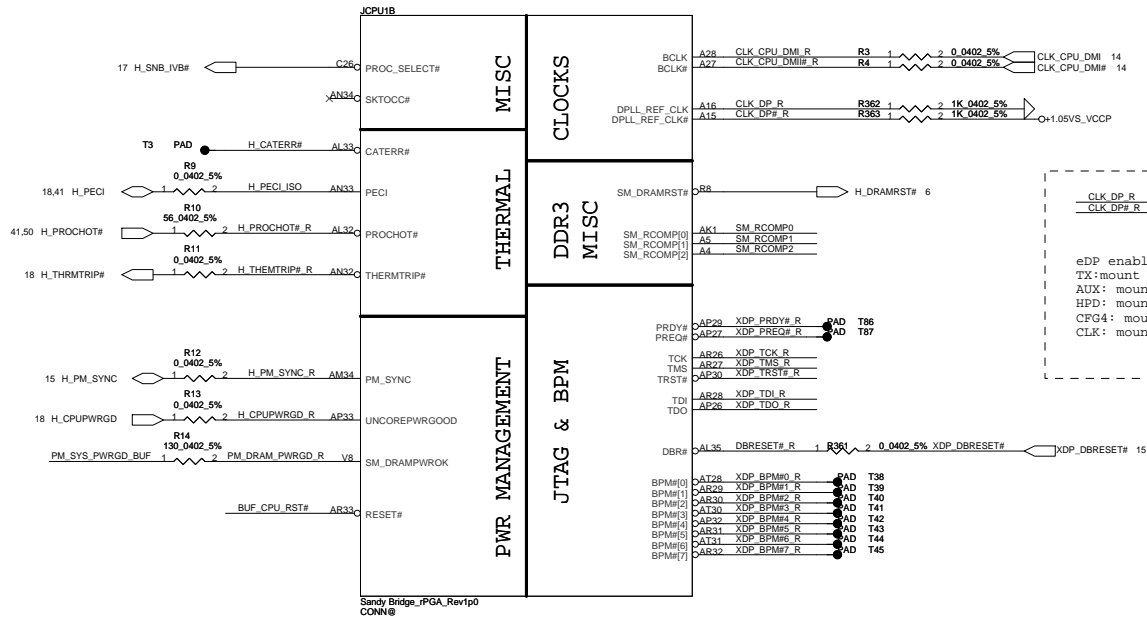
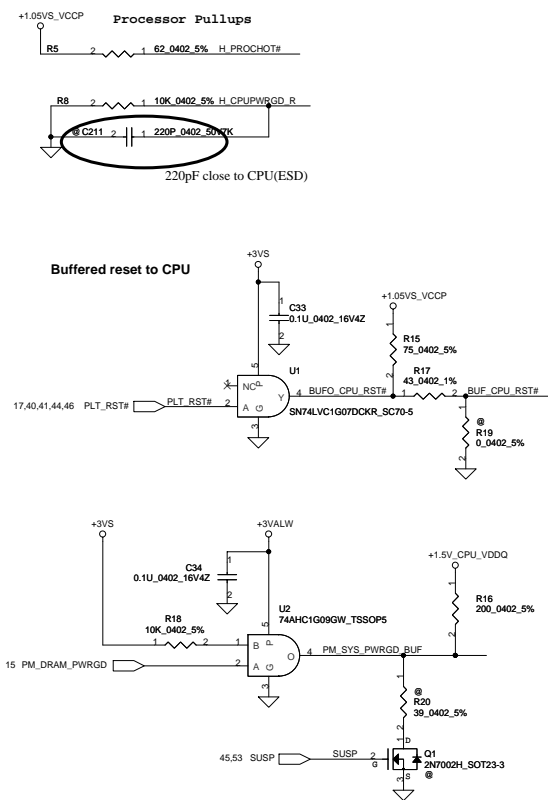
eDP\_COMPPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



INTEL\_RPGA\_989P-S

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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INETL\_RPGA\_989P-S

CLK\_DP\_R R6 1 2 0.0402.5%

CLK\_DP#\_R R7 1 2 0.0402.5%

CLK\_DP 14

CLK\_DP# 14

eDP enable:

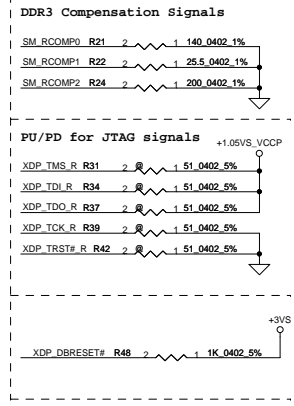
TX: mount C2114, C2115,

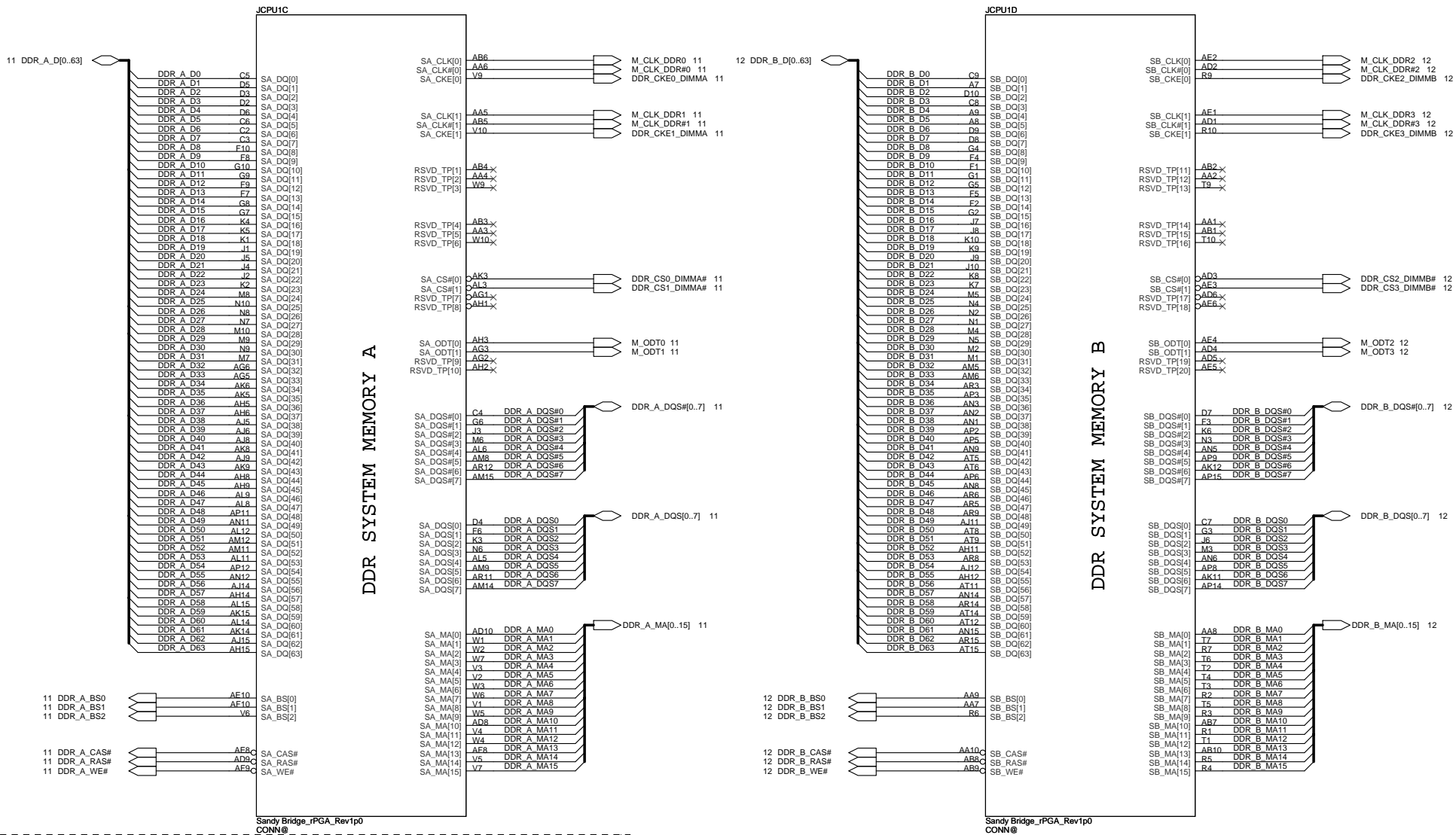
AUX: mount C2118, C2119

HPD: mount R2112, Q2103, R2114

CFG4: mount R55

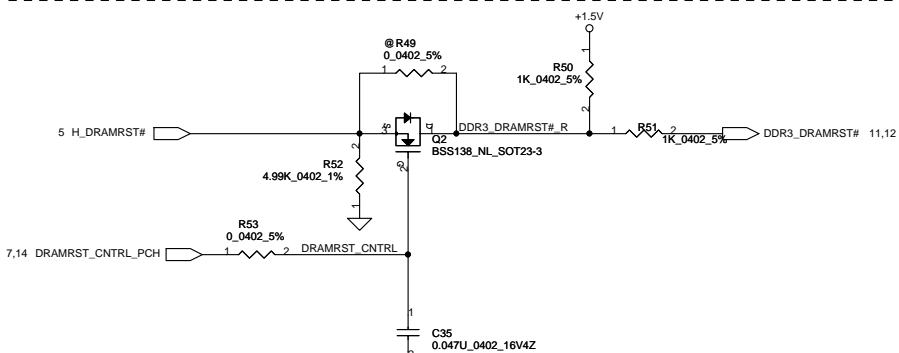
CLK: mount R6, R7, unmount R362, R363



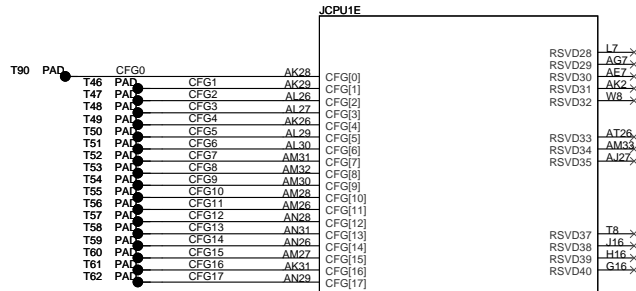


Sandy Bridge\_rPGA\_Rev1p0  
CONN@

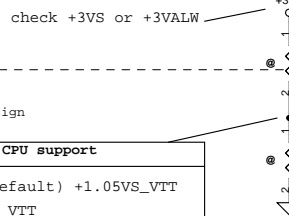
Sandy Bridge\_rPGA\_Rev1p0  
CONN@



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**SA\_DIMM\_VREFDQ**  
**SB\_DIMM\_VREFDQ**  
For Future CPU M3 support,  
Sandy bridge not support M3,  
Check list1.0&CRB say can NC



VCCIO_SEL For 2012 CPU support	
A19	★ 1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

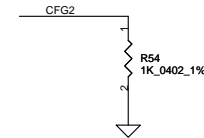
RSVD26 had changed the name to VCCIO\_SEL  
Need PH +3VALW 10K at +1.05VS\_VTT source  
for 2012 processor +1.05V and +1.0V select

**RESERVED**

Sandy Bridge\_rPGA\_Rev1p0  
CONN@

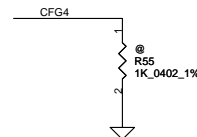
**INTEL\_RPGA\_989P-S**

## CFG Straps for Processor



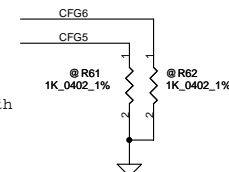
**PEG Static Lane Reversal - CFG2 is for the 16x**

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed
------	--



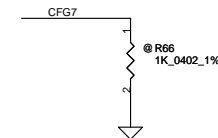
**Display Port Presence Strap**

CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--



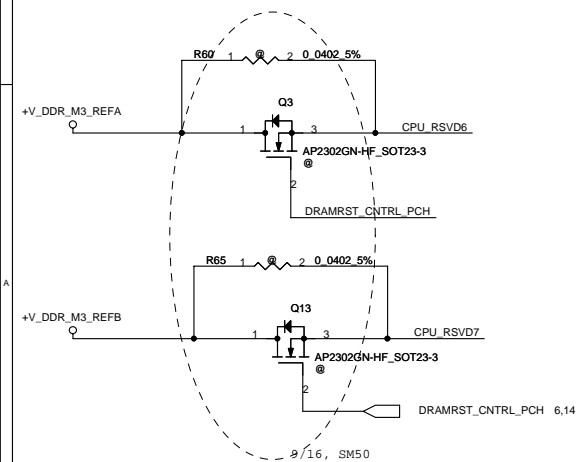
**PCIE Port Bifurcation Straps**

CFG[6:5]	★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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**PEG DEFER TRAINING**

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---

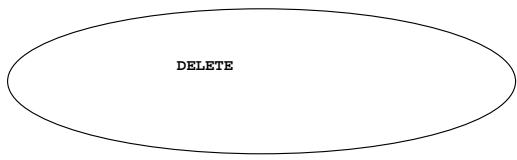


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**SCHEMATIC\_MB LA-A7121**







EDS1.3

## POWER

JCPU1G

+V GFX\_CORE

### Top Socket Cavity

### Top Socket Edge

### Bottom Socket Cavity

### Bottom Socket Edge

### Bottom Socket Edge

QC DC 33A

AT24

AT23

AT21

AT20

AT18

AT17

AT16

AT15

AT14

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AT12

AT11

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AT8

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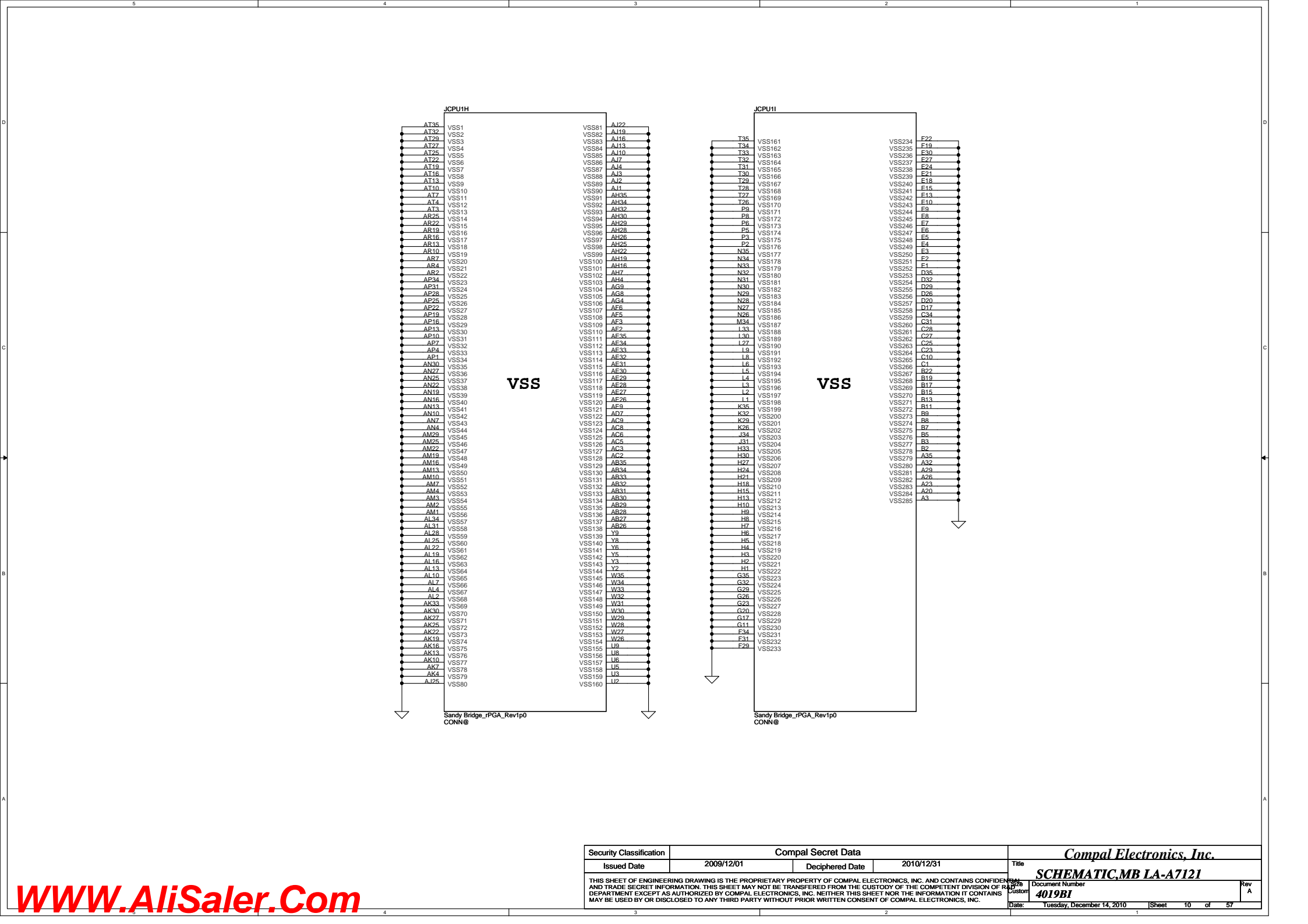
AT-279

AT-280

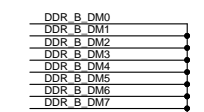
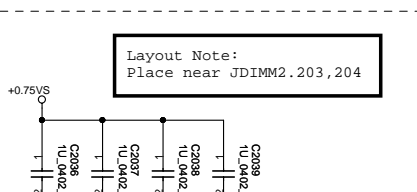
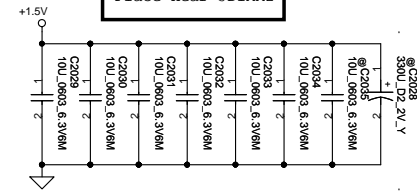
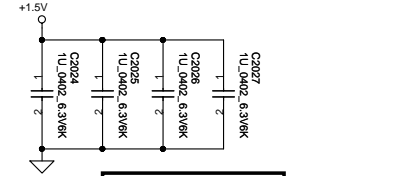
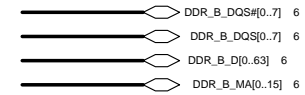
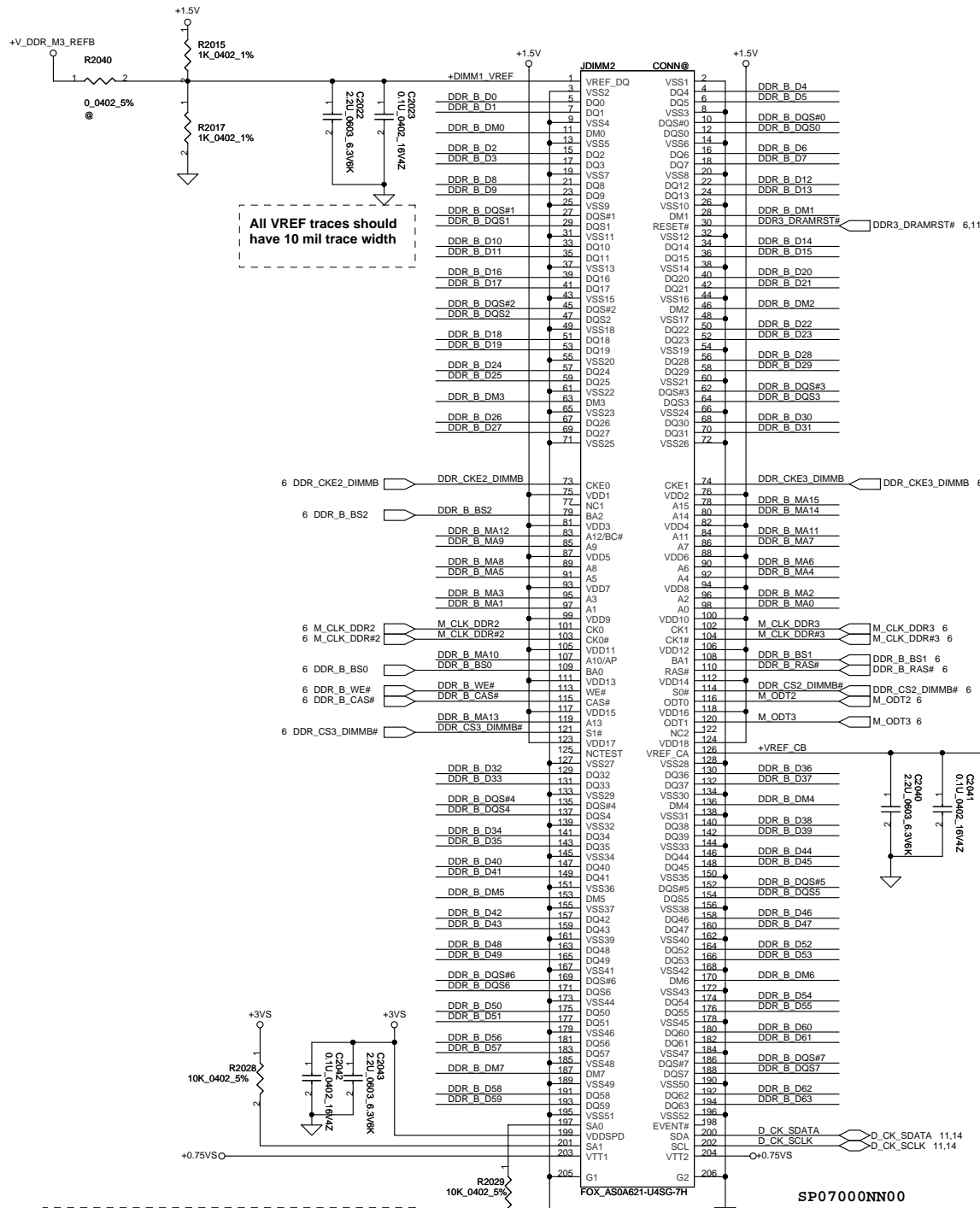
AT-281

AT-282

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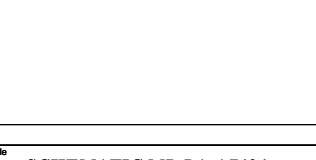
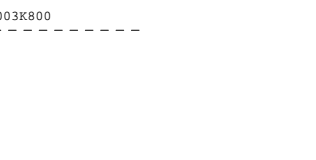
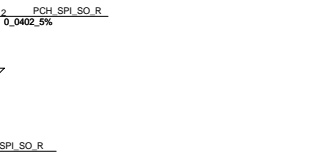
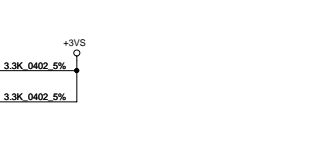
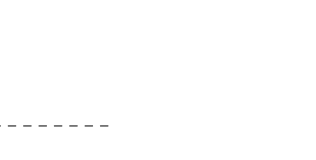
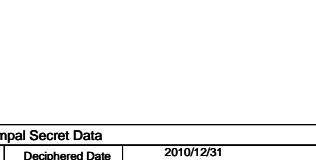
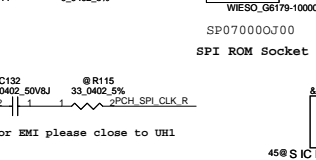
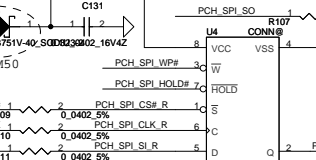
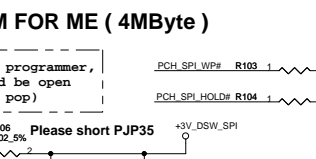
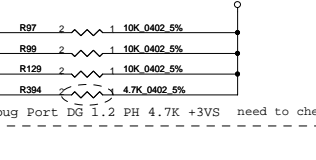
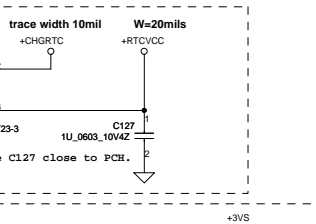
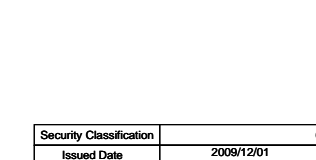
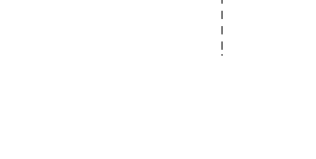
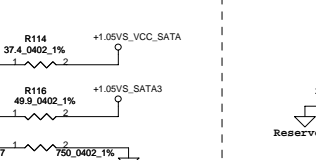
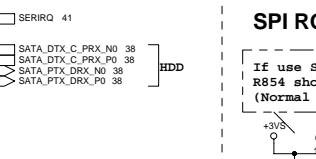
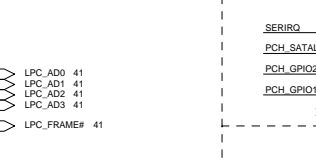
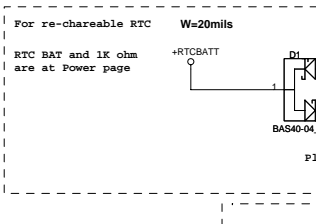
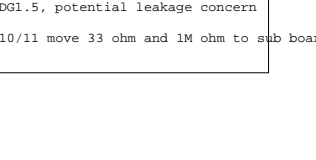
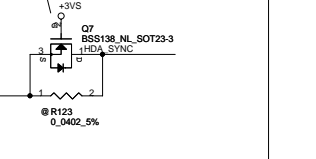
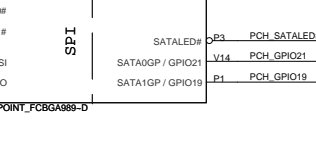
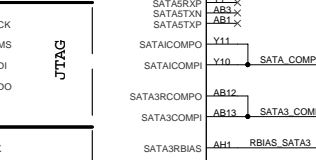
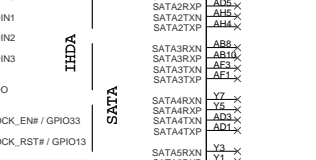
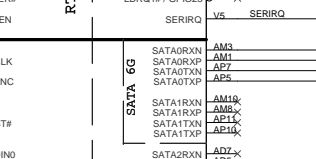
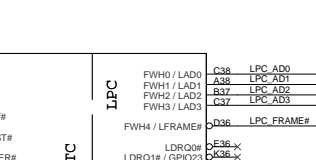
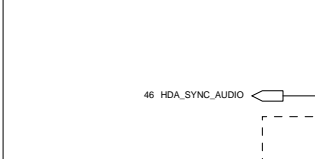
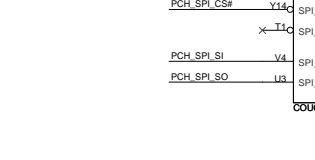
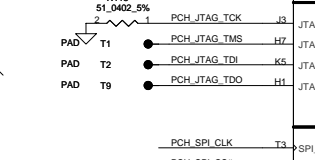
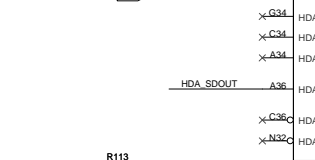
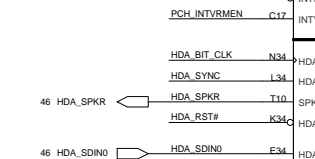
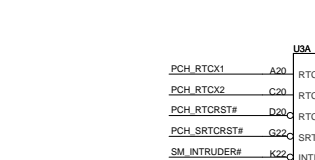
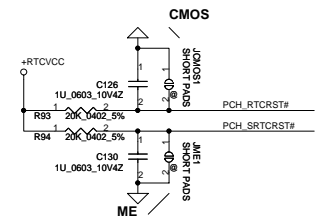
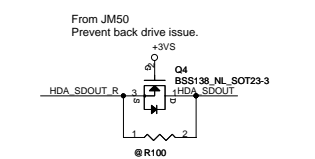
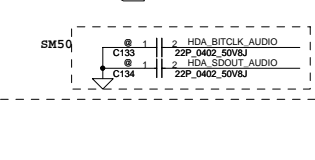
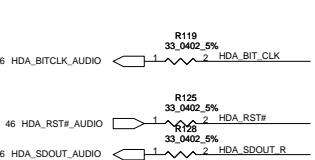
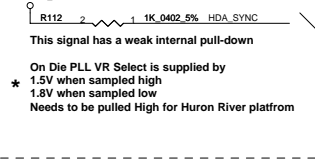
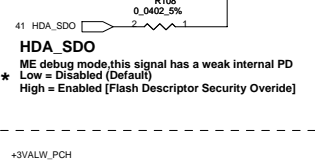
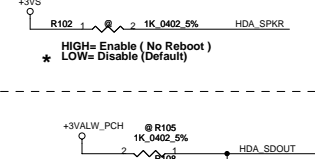
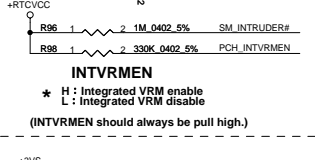
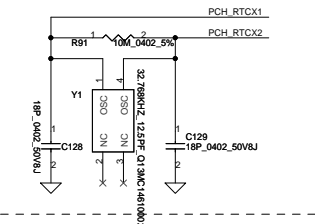


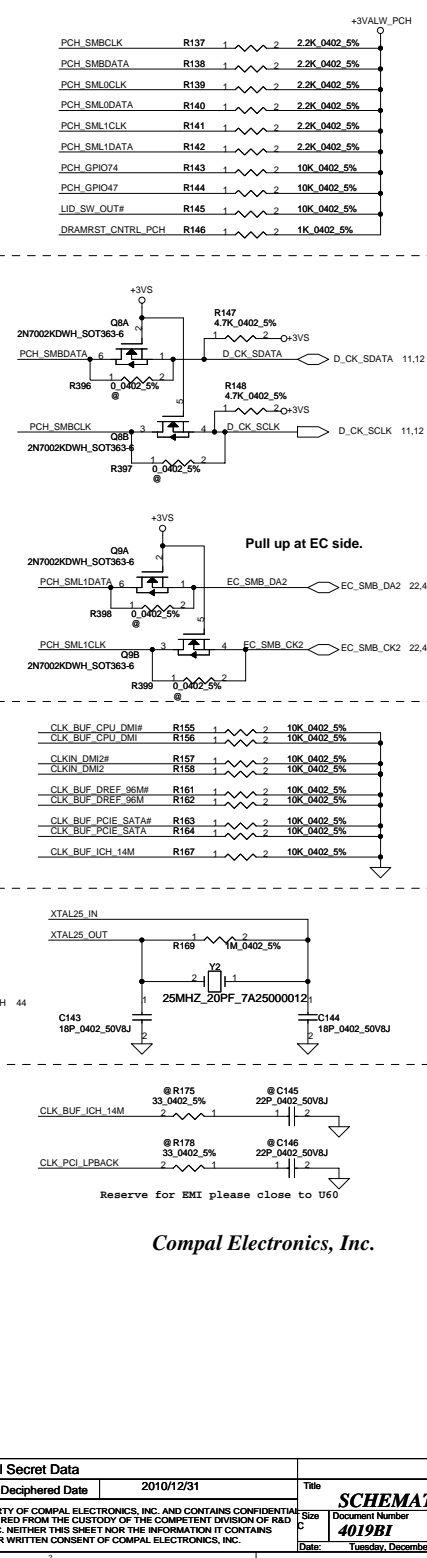
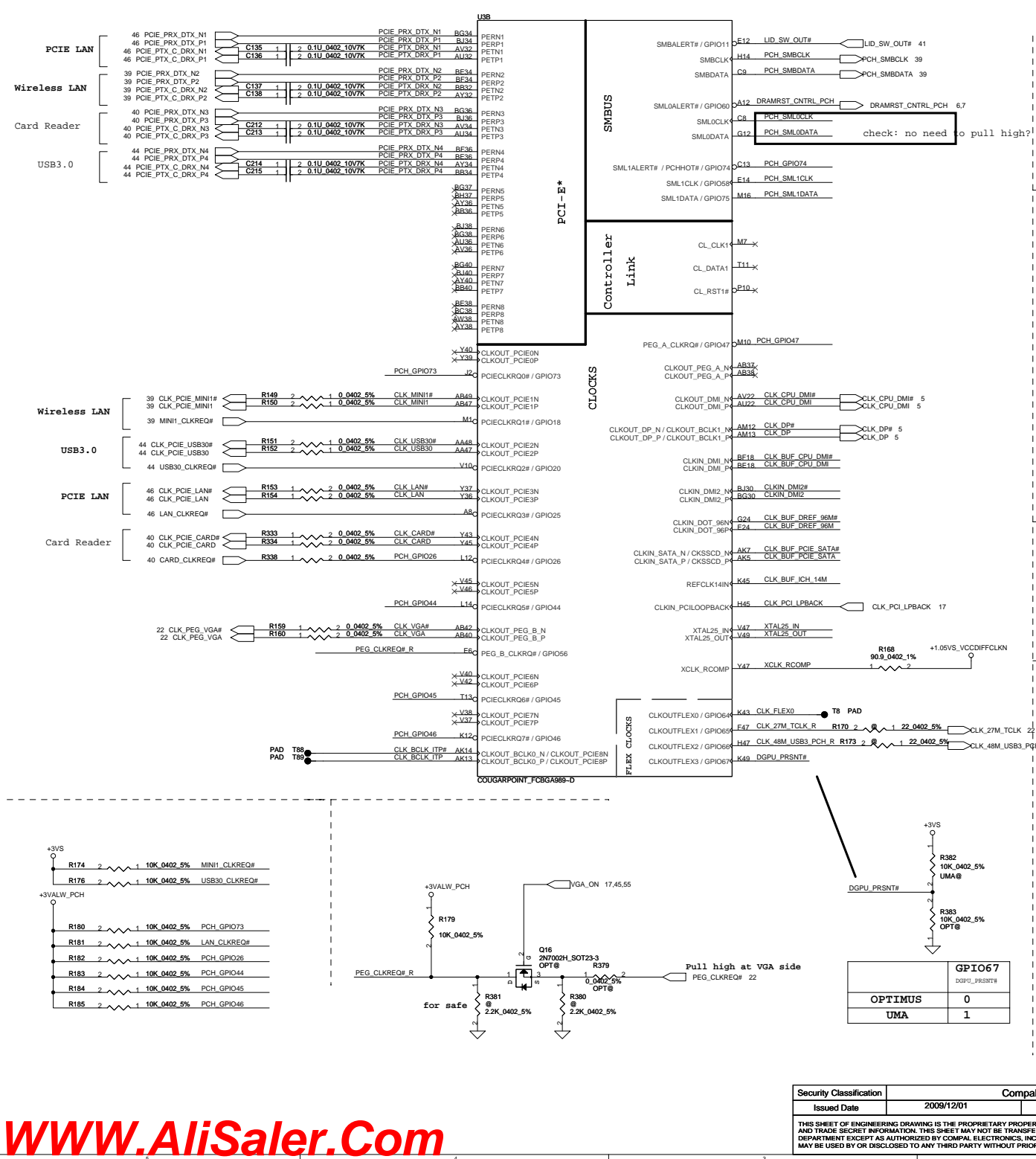


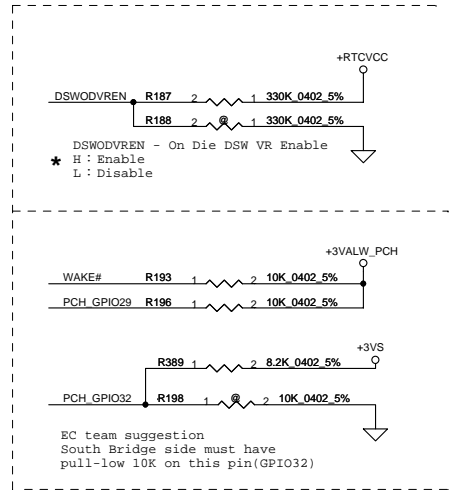
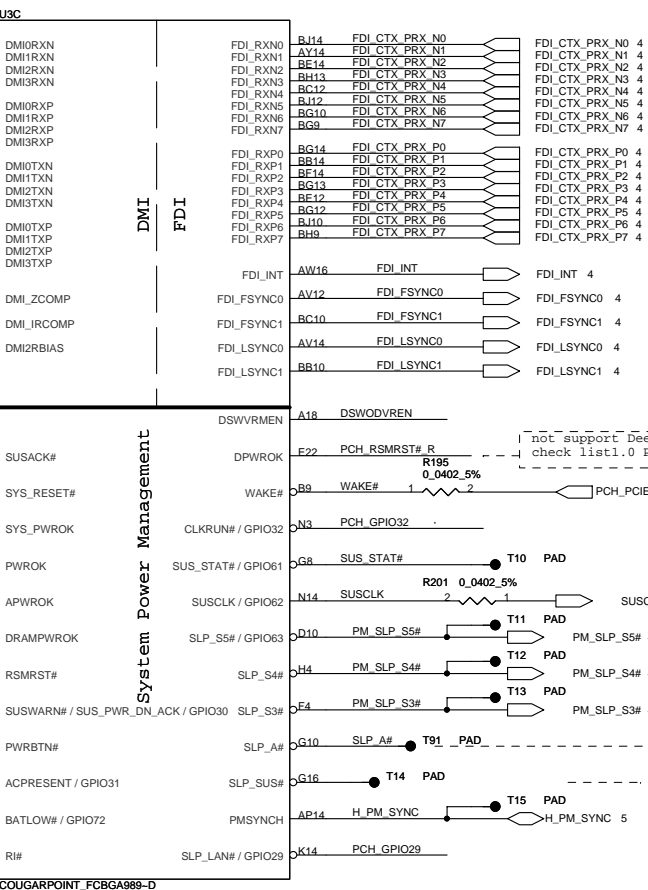
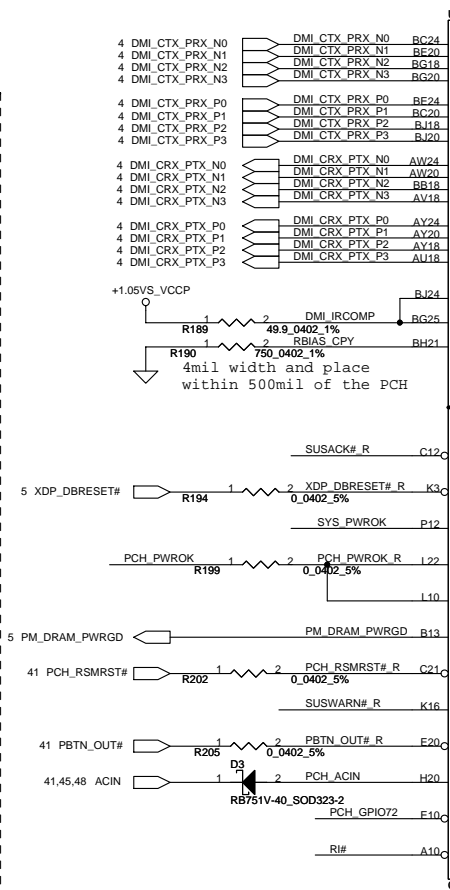
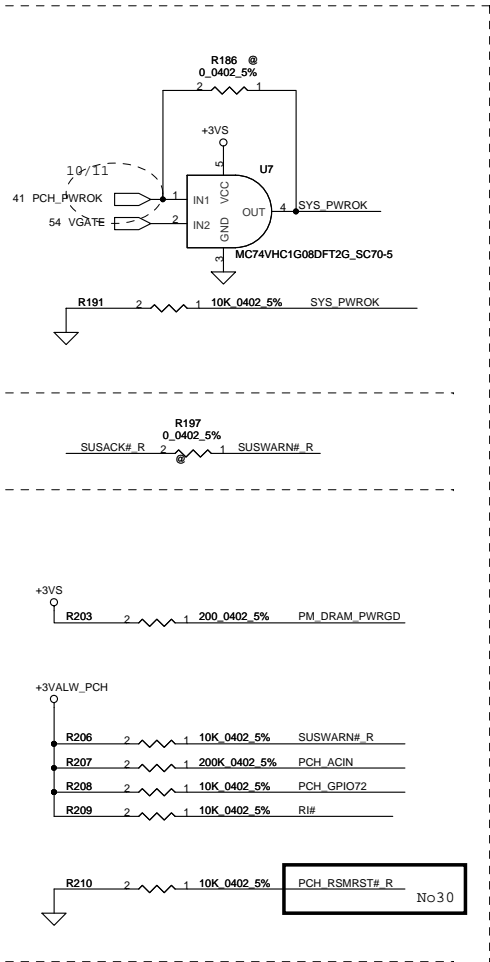
<Address: 01>  
DIMM\_B Standard type H:4mm

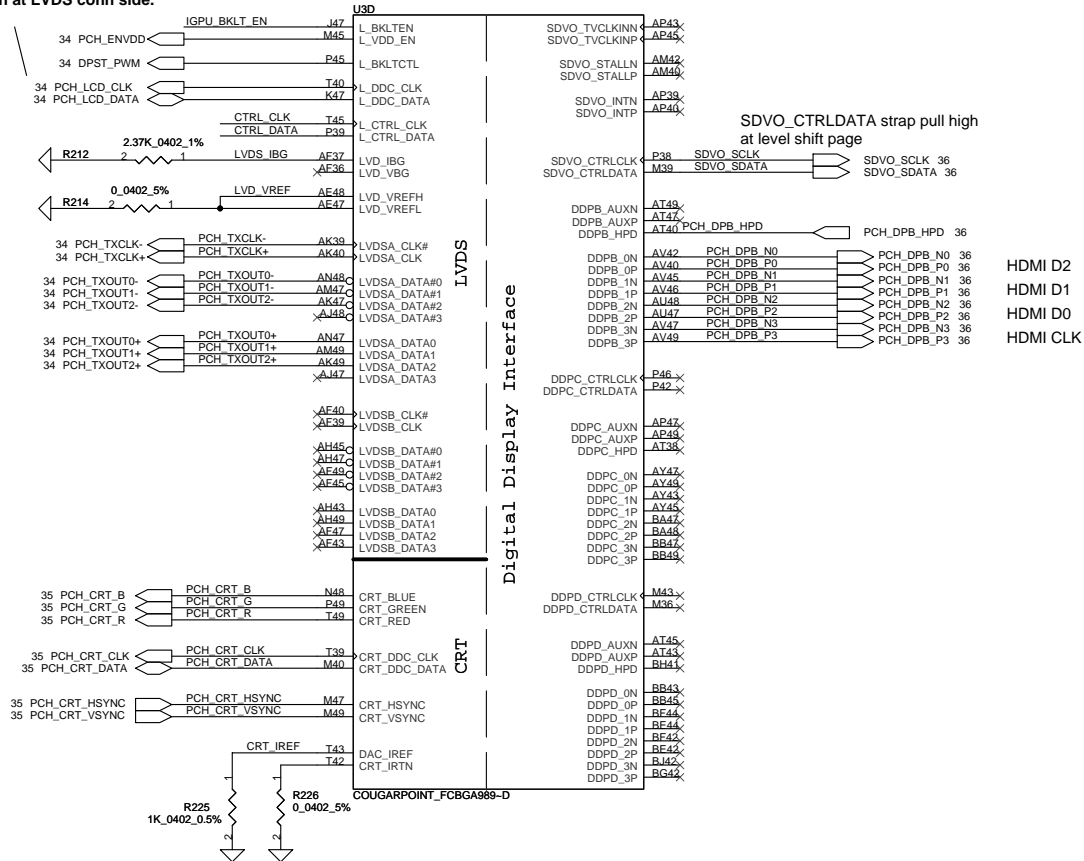
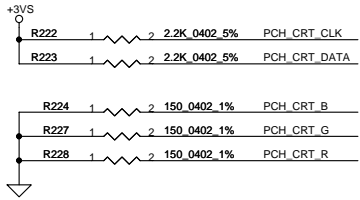
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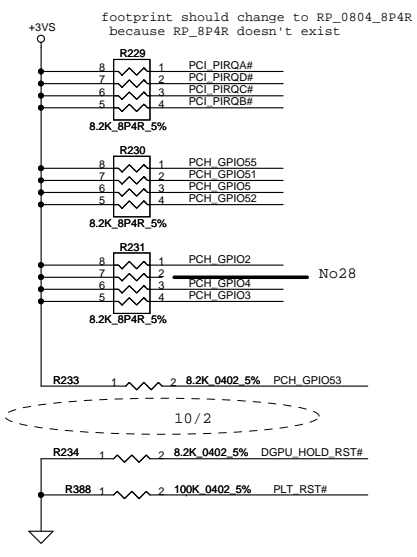




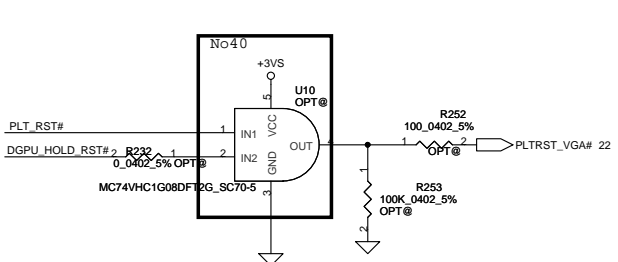
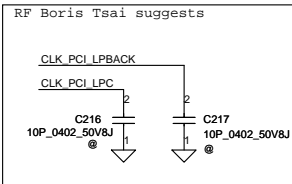




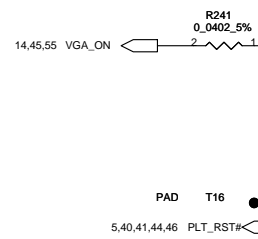




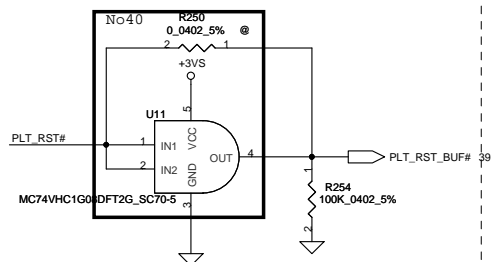
Boot BIOS Strap bit1 BBS1			
		Boot BIOS Destination	
	Bit11	Bit10	
GNT1# / GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC



PCI	
PCI_PIRQA#	K40
PCI_PIRQB#	K38
PCI_PIROC#	H38
PCI_PIROD#	G38
DGPU_HOLD_RST#	C46
PCH_GPIO52	C46
VGA_ON_R	E40
PCH_GPIO51	D47
PCH_GPIO53	E42
PCH_GPIO55	F46
PCH_GPIO2	G42
PCH_GPIO3	G40
PCH_GPIO4	C42
PCH_GPIO5	D44



PCI	
PIRQA#	K40
PIRQB#	K38
PIROC#	H38
PIROD#	G38
REQ1# / GPIO50	C46
REQ2# / GPIO52	C46
REQ3# / GPIO54	E40
GNT1# / GPIO51	D47
GNT2# / GPIO53	E42
GNT3# / GPIO55	F46
PIRQE# / GPIO2	G42
PIRQ# / GPIO3	G40
PIRQG# / GPIO4	C42
PIRQH# / GPIO5	D44



USE		NVRAM		RSVD		PCI		USB	
BG26	TP1	NV_CE#0	AV7	NV_ALE	AV5	PIRQA#	K40	USBP0N	C24
B426	TP2	NV_CE#1	AV7	NV_CLE	AY1	PIRQB#	K38	USBP0P	A24
B425	TP3	NV_CE#2	AV3			PIROC#	H38	USBP1N	C25
B416	TP4	NV_CE#3	BG4			PIROD#	G38	USBP1P	B25
BG16	TP5	NV_DQ#0	AT10	NV_RCOMP	AV10			USBP2N	C26
AH38	TP6	NV_DQ#1	BC8	NV_RB#	AT8			USBP2P	A26
AH37	TP7	NV_DQ#2	AU2	NV_RE#_WRB0	AY5			USBP3N	K28
AK43	TP8	NV_DQ#3	AT4	NV_RE#_WRB1	BA2			USBP3P	H28
AK37	TP9	NV_DQ#4	AT3					USBP4N	E28
C18	TP10	NV_DQ#5	AT1					USBP4P	D28
N30	TP11	NV_DQ#6	AY3					USBP5N	C28
H3	TP12	NV_DQ#7	AT5					USBP5P	A28
AH12	TP13	NV_DQ#8	AV3					USBP6N	C29
AM4	TP14	NV_DQ#9	AV1					USBP6P	B29
AM5	TP15	NV_DQ#10	BB1					USBP7N	N28
Y13	TP16	NV_DQ#11	BA3					USBP7P	K28
K24	TP17	NV_DQ#12	BB5					USBP8N	L28
L24	TP18	NV_DQ#13	BB3					USBP8P	K30
AB46	TP19	NV_DQ#14	BB7					USBP9N	G30
AB45	TP20	NV_DQ#15	BB9					USBP9P	F30
			BD4					USBP10N	C30
			BF6					USBP10P	A30
								USBP11N	L32
								USBP11P	K32
								USBP12N	G32
								USBP12P	F32
								USBP13N	C32
								USBP13P	A32



USB conn (left)  
USB conn (left)

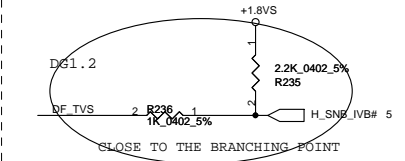
PCI HM65 config not support USB port 6 & 7.

Mini Card(WLAN)  
Mini Card(WWAN)  
CMOS Camera (LVDS)  
Mini Card(SIM reserved)  
Bluetooth



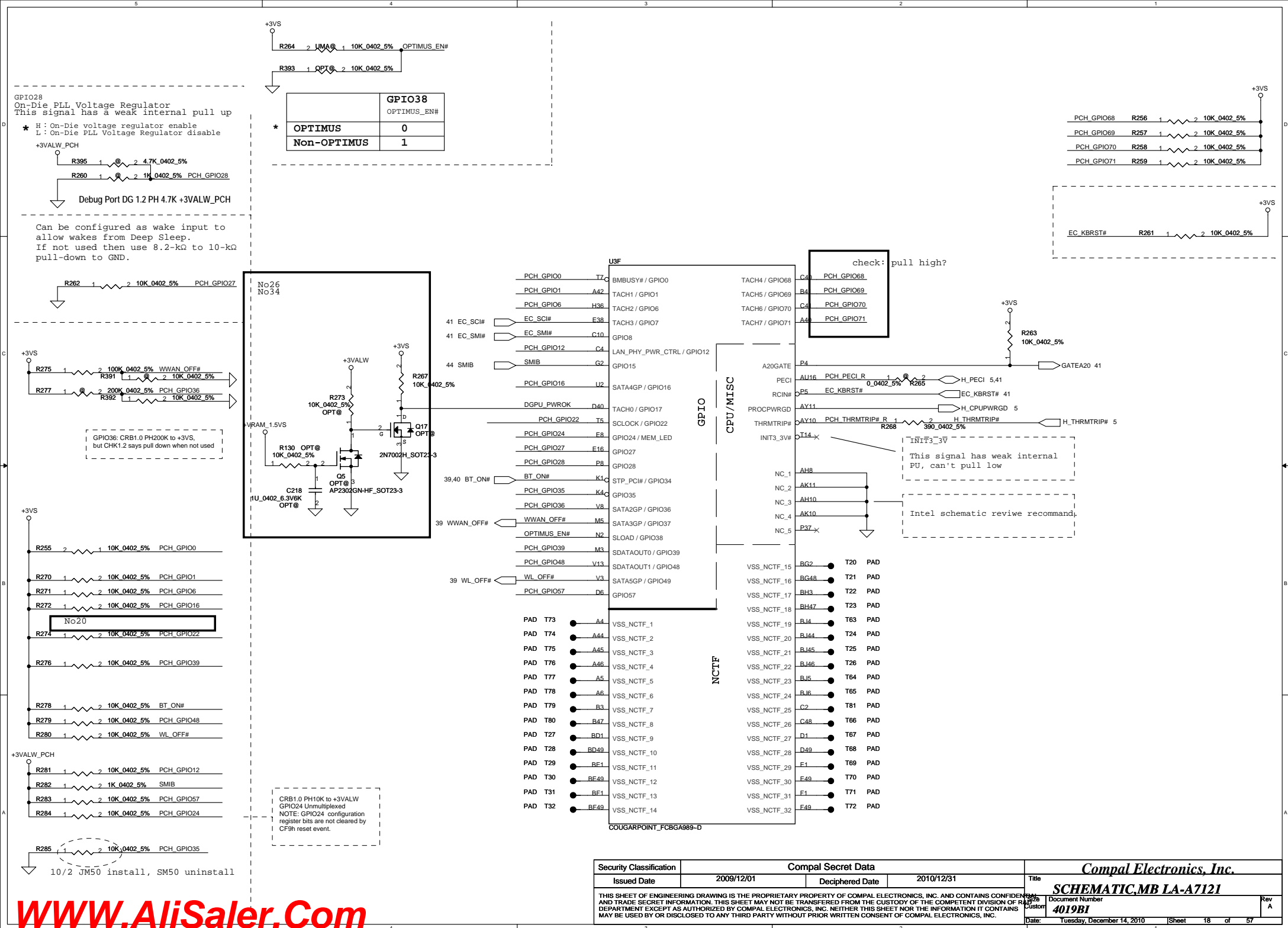
Within 500 mils  
R246 22.6 0402 1%

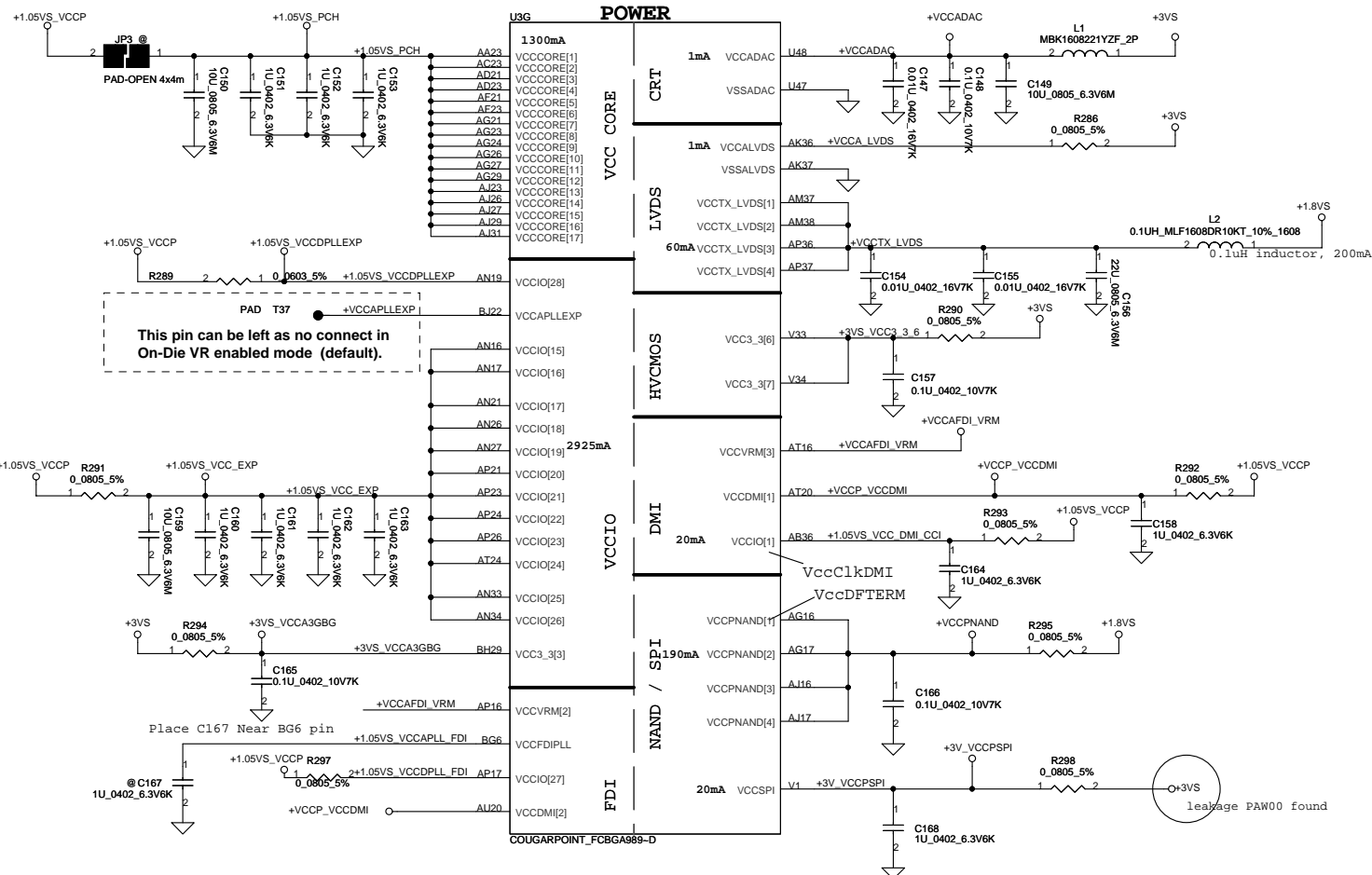
DMI Termination Voltage	
DF_TVS	Set to Vcc when HIGH
	Set to Vss when LOW



USB	
USB_OC0#	R237
USB_OC1#	R238
USB_OC2#	R239
USB_OC3#	R240
USB_OC4#	R242
USB_OC5#	R243
USB_OC6#	R244
USB_OC7#	R245

OC[0..3] use for EHCI 1  
OC[4..7] use for EHCI 2





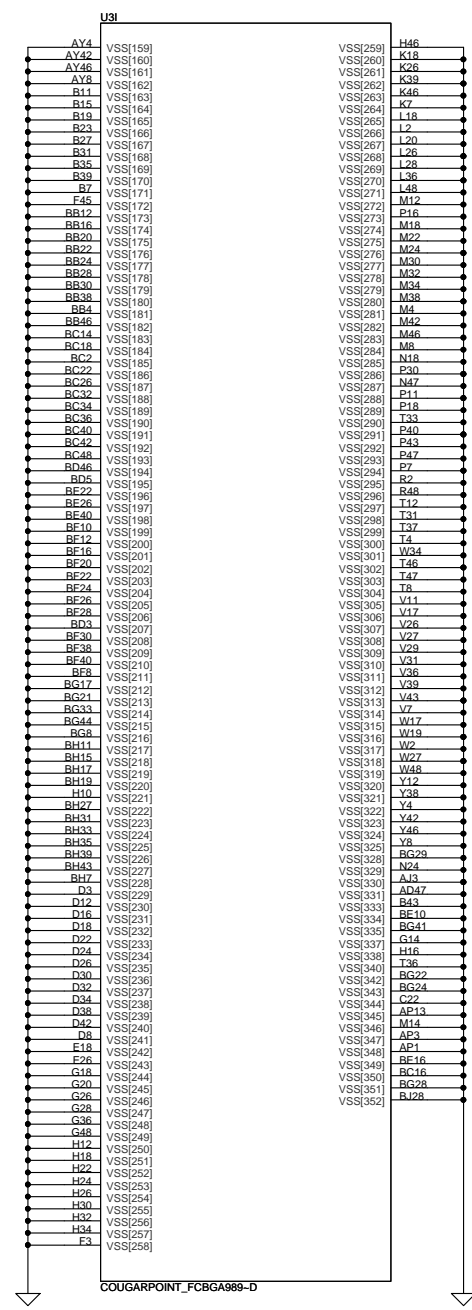
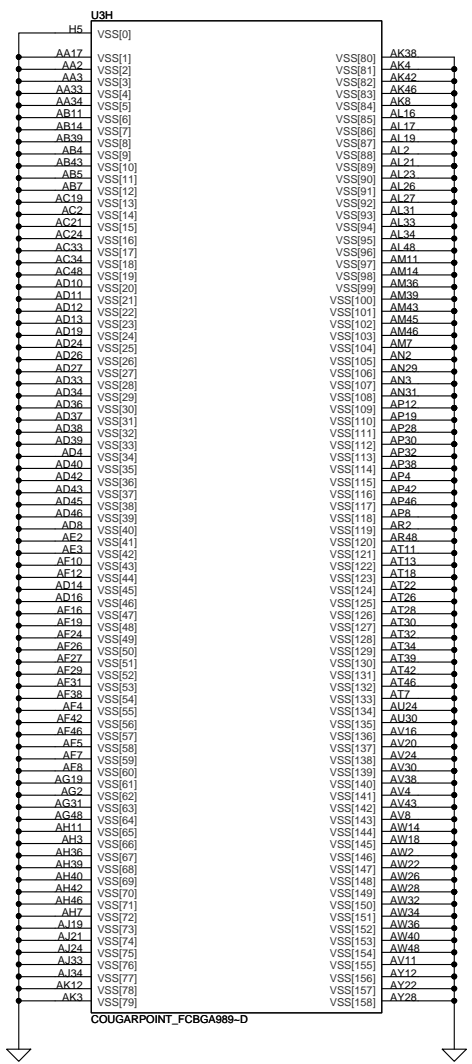
PCH Power Rail Table		
Voltage Rail	Voltage	60 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

+1.5VS  
 R299 2 0.0603.5% +VCCAFDI\_VRM  
 +VCCAFDI\_VRM  
 VCCVRM==>1.5V FOR MOBILE  
 VCCVRM==>1.8V FOR DESKTOP  
 VCCVRM = 160mA detail waiting for newest spec

0 ohm for current test: delete when phase B

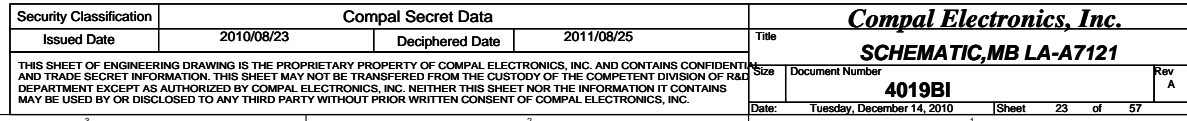
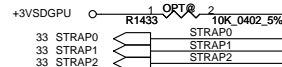
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## For PHQAA EVT Phase only

Mode	VID1	VID0	+VGA_CORE
P0(Cold)	1	1	0.95 V
P0	0	1	0.950V
P8/P12	0	0	0.825 V

## N12M-GE Performance Mode

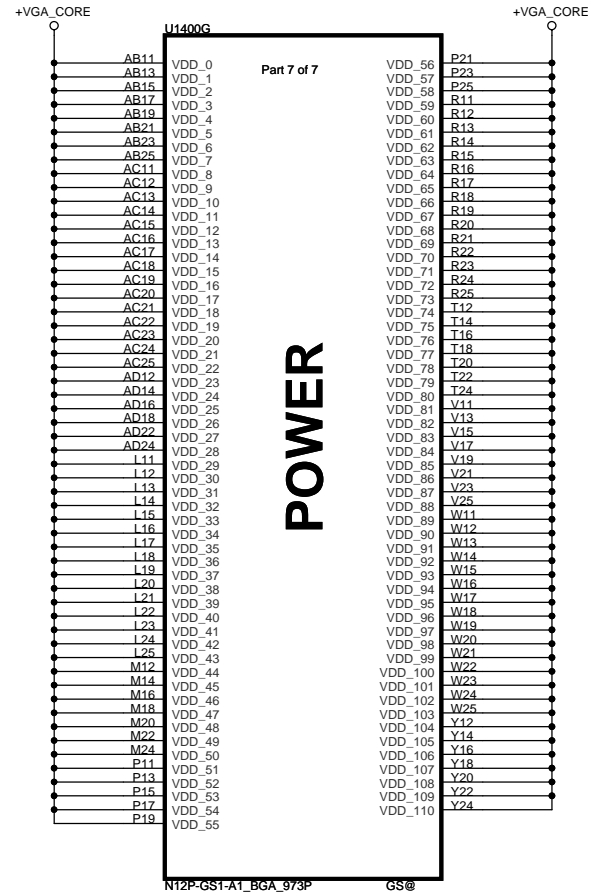
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	606	790	1.00 V
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

## N12P-GS Performance Mode

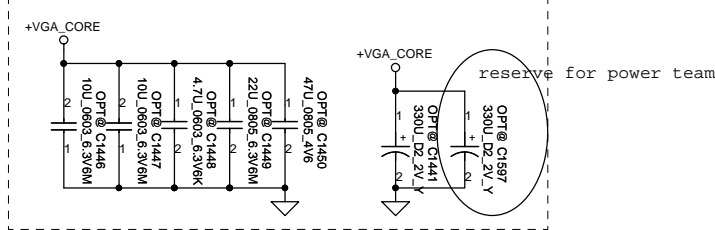
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

## N12P-GE Performance Mode

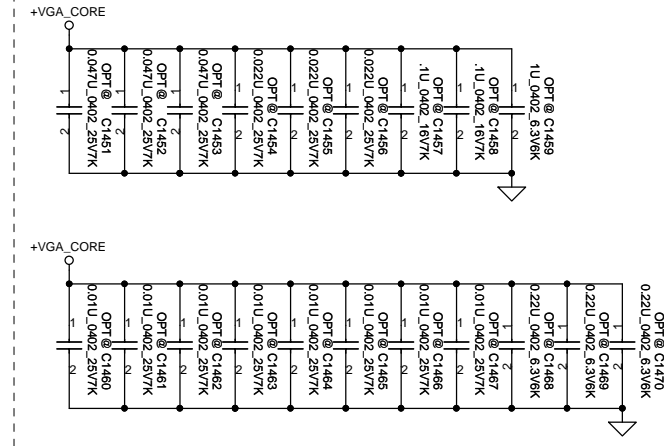
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD



Layout note: Near GPU



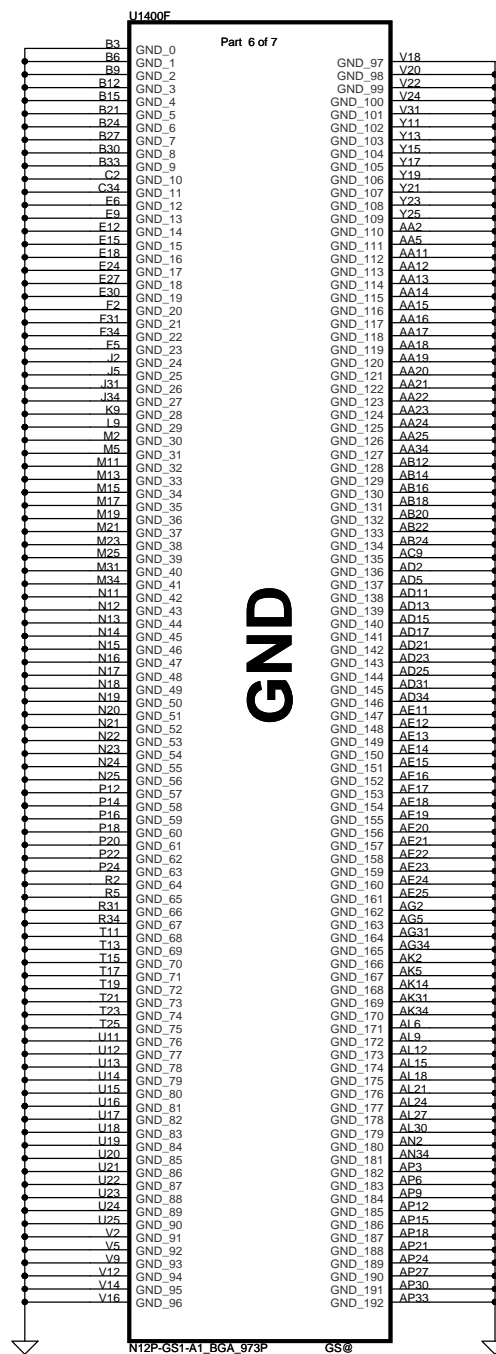
Layout note: Under GPU



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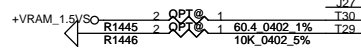
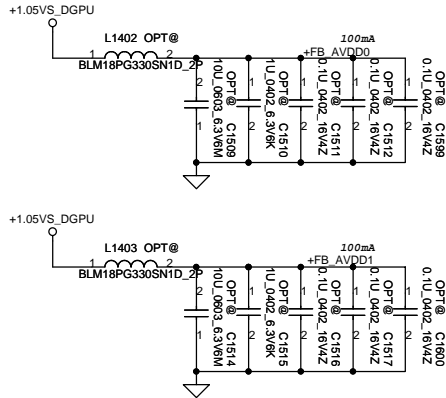






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29.30 MDA[0..63] ← MDA[0..63]



U1400B	
Part 2 of 7	
MDA0	L32 FBA_D0
MDA1	N33 FBA_D1
MDA2	L33 FBA_D2
MDA3	N34 FBA_D3
MDA4	N35 FBA_D4
MDA5	P35 FBA_D5
MDA6	P33 FBA_D6
MDA7	P34 FBA_D7
MDA8	K35 FBA_D8
MDA9	K34 FBA_D9
MDA10	K34 FBA_D10
MDA11	L33 FBA_D11
MDA12	G34 FBA_D12
MDA13	G33 FBA_D13
MDA14	E34 FBA_D14
MDA15	E33 FBA_D15
MDA16	G31 FBA_D16
MDA17	F30 FBA_D17
MDA18	G30 FBA_D18
MDA19	G32 FBA_D19
MDA20	K30 FBA_D20
MDA21	K32 FBA_D21
MDA22	K34 FBA_D22
MDA23	K31 FBA_D23
MDA24	L31 FBA_D24
MDA25	L30 FBA_D25
MDA26	M32 FBA_D26
MDA27	N30 FBA_D27
MDA28	M30 FBA_D28
MDA29	P31 FBA_D29
MDA30	R32 FBA_D30
MDA31	R30 FBA_D31
MDA32	AG30 FBA_D32
MDA33	AG32 FBA_D33
MDA34	AH31 FBA_D34
MDA35	AE31 FBA_D35
MDA36	AE30 FBA_D36
MDA37	AE30 FBA_D37
MDA38	AC32 FBA_D38
MDA39	AD30 FBA_D39
MDA40	AN33 FBA_D40
MDA41	AL31 FBA_D41
MDA42	AM33 FBA_D42
MDA43	AL33 FBA_D43
MDA44	AK30 FBA_D44
MDA45	AK32 FBA_D45
MDA46	AI30 FBA_D46
MDA47	AH30 FBA_D47
MDA48	AH33 FBA_D48
MDA49	AH35 FBA_D49
MDA50	AH34 FBA_D50
MDA51	AH32 FBA_D51
MDA52	AI33 FBA_D52
MDA53	AI35 FBA_D53
MDA54	AM34 FBA_D54
MDA55	AM35 FBA_D55
MDA56	AE33 FBA_D56
MDA57	AE32 FBA_D57
MDA58	AF34 FBA_D58
MDA59	AE35 FBA_D59
MDA60	AE34 FBA_D60
MDA61	AE33 FBA_D61
MDA62	AB32 FBA_D62
MDA63	AC35 FBA_D63
+FB AVDD0 AG27 FB_DLLAVDD_0 AF27 FB_PLLAVDD_0	
+FB AVDD1 J19 FB_DLLAVDD_1 J18 FB_PLLAVDD_1	
FB_VREF NC T30 FBA_DEBUG0 T29 FBA_DEBUG1	
+VRAM_1.5V R1445 2 OPT@ 1 60.4 0402 1% R1446 2 OPT@ 1 10K 0402 5%	

MEMORY INTERFACE

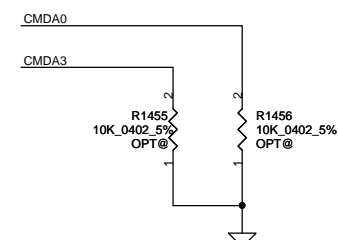
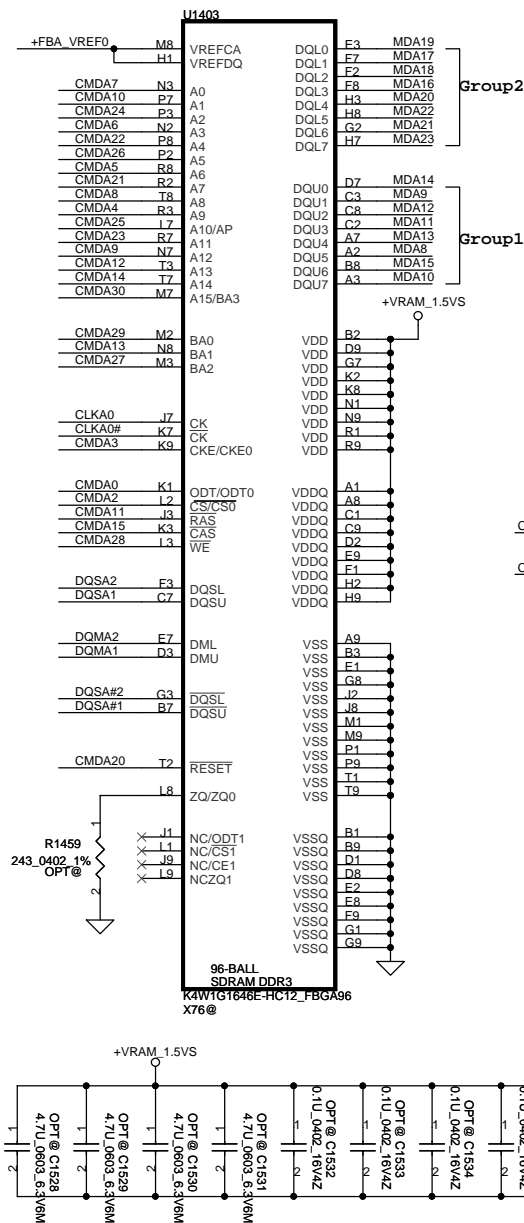
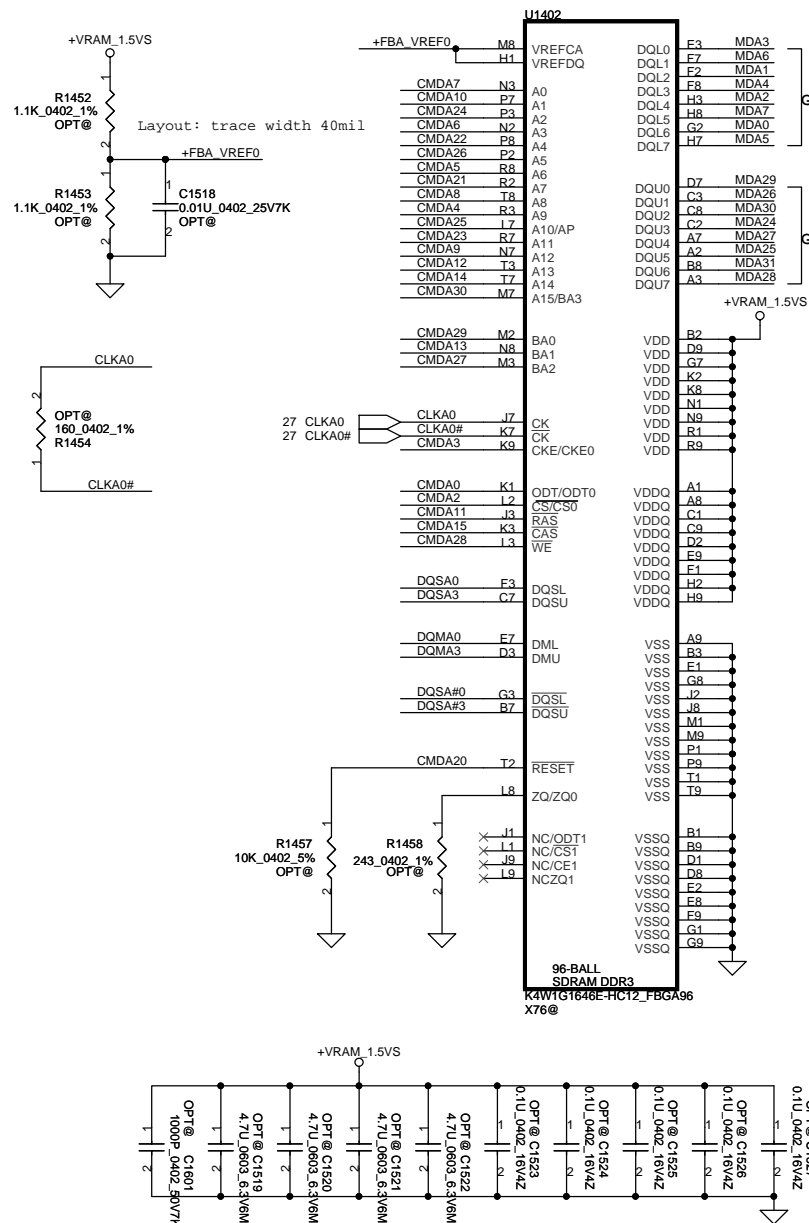
FBA_CMD0	U30 CMDA0	CMDA0 29
FBA_CMD1	U31 CMDA2	CMDA2 29
FBA_CMD2	V32 CMDA3	CMDA3 29
FBA_CMD3	T35 CMDA4	CMDA4 29,30
FBA_CMD4	V32 CMDA5	CMDA5 29,30
FBA_CMD5	W33 CMDA7	CMDA6 29,30
FBA_CMD6	W33 CMDA8	CMDA7 29,30
FBA_CMD7	W31 CMDA8	CMDA8 29,30
FBA_CMD8	W34 CMDA9	CMDA9 29,30
FBA_CMD9	U34 CMDA10	CMDA10 29,30
FBA_CMD10	U35 CMDA11	CMDA11 29,30
FBA_CMD11	U32 CMDA12	CMDA12 29,30
FBA_CMD12	T34 CMDA13	CMDA13 29,30
FBA_CMD13	T33 CMDA14	CMDA14 29,30
FBA_CMD14	W30 CMDA15	CMDA15 29,30
FBA_CMD15	AB30 CMDA16	CMDA16 30
FBA_CMD16	AA31 CMDA18	CMDA18 30
FBA_CMD17	AB31 CMDA19	CMDA19 30
FBA_CMD18	AA32 CMDA20	CMDA20 29,30
FBA_CMD19	AB33 CMDA21	CMDA21 29,30
FBA_CMD20	Y32 CMDA22	CMDA22 29,30
FBA_CMD21	Y32 CMDA23	CMDA23 29,30
FBA_CMD22	AB34 CMDA24	CMDA24 29,30
FBA_CMD23	AB35 CMDA25	CMDA25 29,30
FBA_CMD24	Y35 CMDA26	CMDA26 29,30
FBA_CMD25	W35 CMDA27	CMDA27 29,30
FBA_CMD26	Y34 CMDA28	CMDA28 29,30
FBA_CMD27	Y31 CMDA29	CMDA29 29,30
FBA_CMD28	Y30 CMDA30	CMDA30 29,30
FBA_CMD29	W29 CMDA30	CMDA30 29,30
FBA_CMD30	Y29 CMDA30	CMDA30 29,30
FBA_CMD31	Y29 CMDA30	CMDA30 29,30
FBA_CMD32	P32 DQMA0	DQMA[7..0] 29,30
FBA_CMD33	L34 DQMA1	DQSA#[7..0] 29,30
FBA_CMD34	L30 DQMA2	DQSA#[7..0] 29,30
FBA_CMD35	P30 DQMA3	DQSA#[7..0] 29,30
FBA_CMD36	AE32 DQMA4	DQSA#[7..0] 29,30
FBA_CMD37	AL32 DQMA5	DQSA#[7..0] 29,30
FBA_CMD38	AL34 DQMA6	DQSA#[7..0] 29,30
FBA_CMD39	AF35 DQMA7	DQSA#[7..0] 29,30
FBA_CMD40	L35 DQSA#0	DQSA#[7..0] 29,30
FBA_CMD41	G35 DQSA#1	DQSA#[7..0] 29,30
FBA_CMD42	H31 DQSA#2	DQSA#[7..0] 29,30
FBA_CMD43	N32 DQSA#3	DQSA#[7..0] 29,30
FBA_CMD44	AD32 DQSA#4	DQSA#[7..0] 29,30
FBA_CMD45	AI31 DQSA#5	DQSA#[7..0] 29,30
FBA_CMD46	AI35 DQSA#6	DQSA#[7..0] 29,30
FBA_CMD47	AC34 DQSA#7	DQSA#[7..0] 29,30
FBA_CMD48	L34 DQSA0	DQSA0 29
FBA_CMD49	H35 DQSA1	DQSA1 29
FBA_CMD50	J32 DQSA2	DQSA2 29
FBA_CMD51	N31 DQSA3	DQSA3 29
FBA_CMD52	AE31 DQSA4	DQSA4 29
FBA_CMD53	AI32 DQSA5	DQSA5 29
FBA_CMD54	AI34 DQSA6	DQSA6 29
FBA_CMD55	AC33 DQSA7	DQSA7 29
FBA_CMD56	P29 WCK0	WCK0 29
FBA_CMD57	R29 WCK0_N	WCK0_N 29
FBA_CMD58	L29 WCK1	WCK1 29
FBA_CMD59	M29 WCK1_N	WCK1_N 29
FBA_CMD60	AG29 WCK2	WCK2 29
FBA_CMD61	AH29 WCK2_N	WCK2_N 29
FBA_CMD62	AD29 WCK3	WCK3 29
FBA_CMD63	AE29 WCK3_N	WCK3_N 29
FBA_CMD64	T32 CLKA0	CLKA0 29
FBA_CMD65	T31 CLKA0#	CLKA0# 29
FBA_CMD66	AC31 CLKA1	CLKA1 30
FBA_CMD67	AC30 CLKA1#	CLKA1# 30

GB2-128  
Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD5	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



*Memory Partition A - Lower 32 bits*



MDA[0..63]	27,30
CMDA[30..0]	27,30
DQMA[7..0]	27,30
DQSA[7..0]	27,30
DQSA#[7..0]	27,30

GB2-128  
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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Memory Partition A - Upper 32 bits

U1404

U1405

Mode E - Mirror Mode Mapping

Address	DATA	Bus
CMD3	CKE_L	32...63
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification

Compal Secret Data

Issued Date: 2010/08/23

Deciphered Date: 2011/08/25

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Compal Electronics, Inc.

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Rev A

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition C - Lower 32 bits

The diagram illustrates the lower 32 bits of Memory Partition C, featuring two memory modules, U1406 and U1407, each a 96-BALL SDRAM DDR3 (K4W1G1646E-HC12-FBG A96 X76@). The modules are connected to a power supply (+VRAM\_1.5VS) and ground. The schematic shows the pin connections for each module, including address, data, and control signals. The modules are organized into four groups: Group0, Group1, Group2, and Group3. The diagram also includes a memory mapping table for Mode E - Mirror Mode Mapping, showing the mapping of memory addresses to data bus signals. The table is as follows:

Address	DATA Bus
CMD8	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15

GB2-128		
Table E - Mirror Mode Mapping		
	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

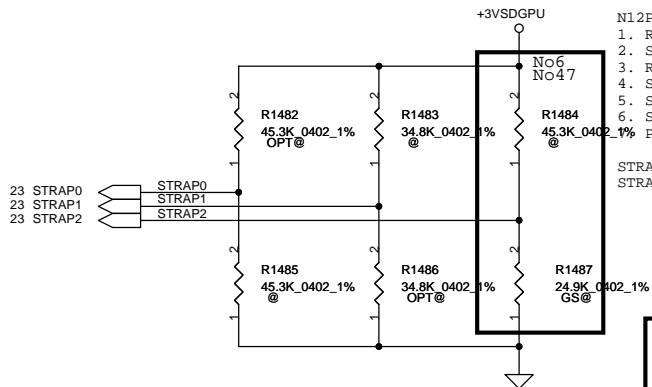
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	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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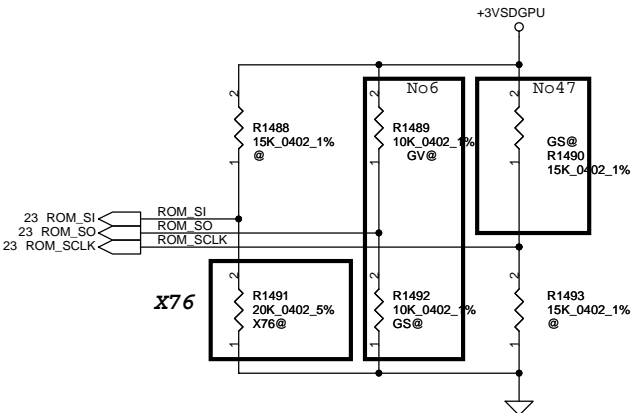
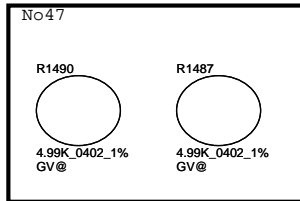




N12P-GV QS DevID: 0x1050,  
1. ROM\_SCLK: pull up 5K ohm.  
2. STRAP2: pull down 5K ohm.  
3. ROM\_SO: pull up 10K ohm.  
4. STRAP3: pull down 5K ohm.  
5. STRAP4: pull down 10K ohm.  
6. STRAP\_REF2, need to stuff with 40K ohm 1%.  
PGOOD (pin E7) stuff 10K ohm.

STRAP0: as same as N12P-GS with 45K pull up.  
STRAP1: pull down 35K as N12P-GS

GV:  
GB1b-64



Option Component



GS:

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

N11P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	L 35K	L GV@ GS@	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	L 35K	L GV@ GS@	L 15K	L 10K	H 15K
128MX16 Samsung	H 45K	L 35K	L GS@	L 45K	L 10K	H 15K
128MX16 Hynix SA00003VS10	H 45K	L 35K	L GS@	L 35K	L 10K	H 15K

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

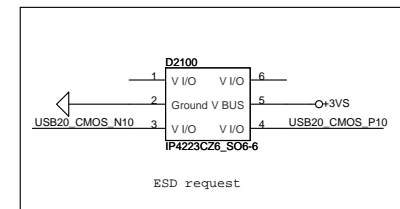
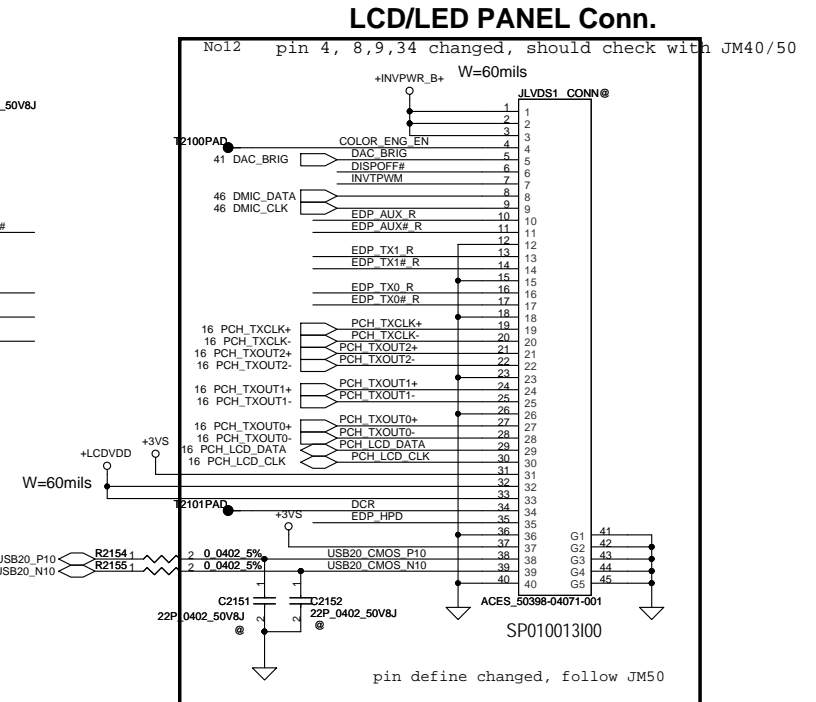
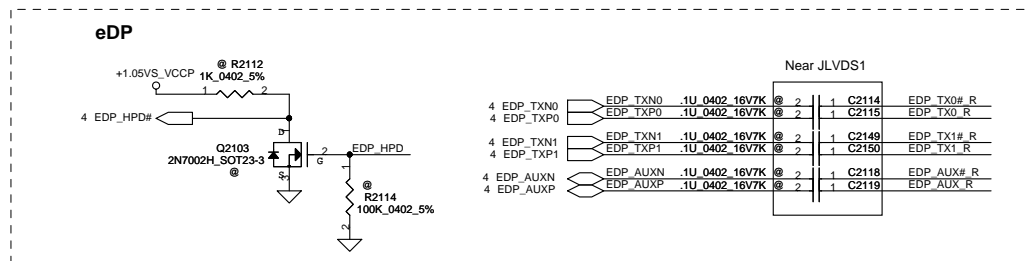
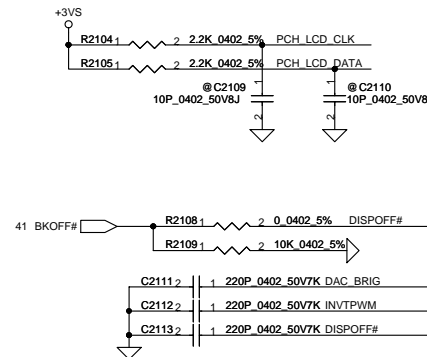
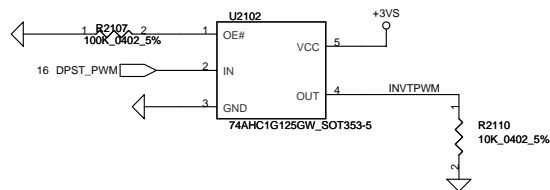
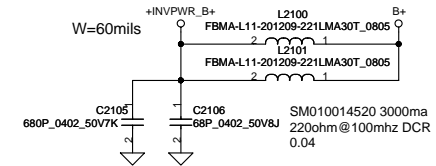
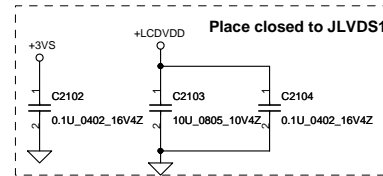
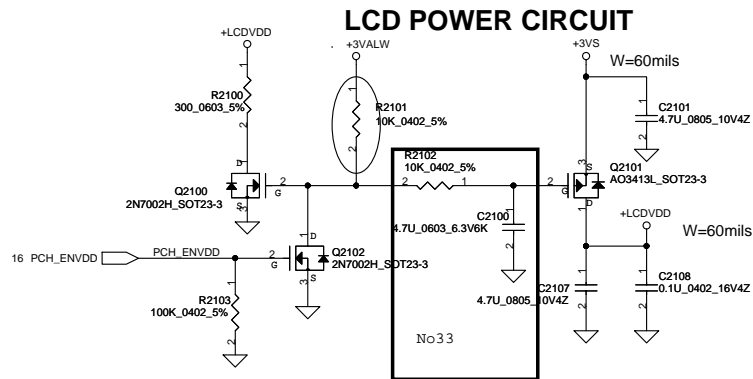
GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K
N12P-GV	0x1050	Pull up 5K	pull down 5K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S40	512MB	0010	PD 15K (SD034150280)
	1GB	0010	PD 15K (SD034150280)
Hynix 2G 128MX16 H5TQ2G63BFR-12C SA00003YO20	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646G-BC11 SA00004GS10	512MB	0011	PD 20K (SD034200280)
	1GB	0011	PD 20K (SD034200280)
Samsung 2G 128M16 K4W2G1646C-HC12 SA000047Q20	2GB	0111	PD 45.3K(SD034453280)

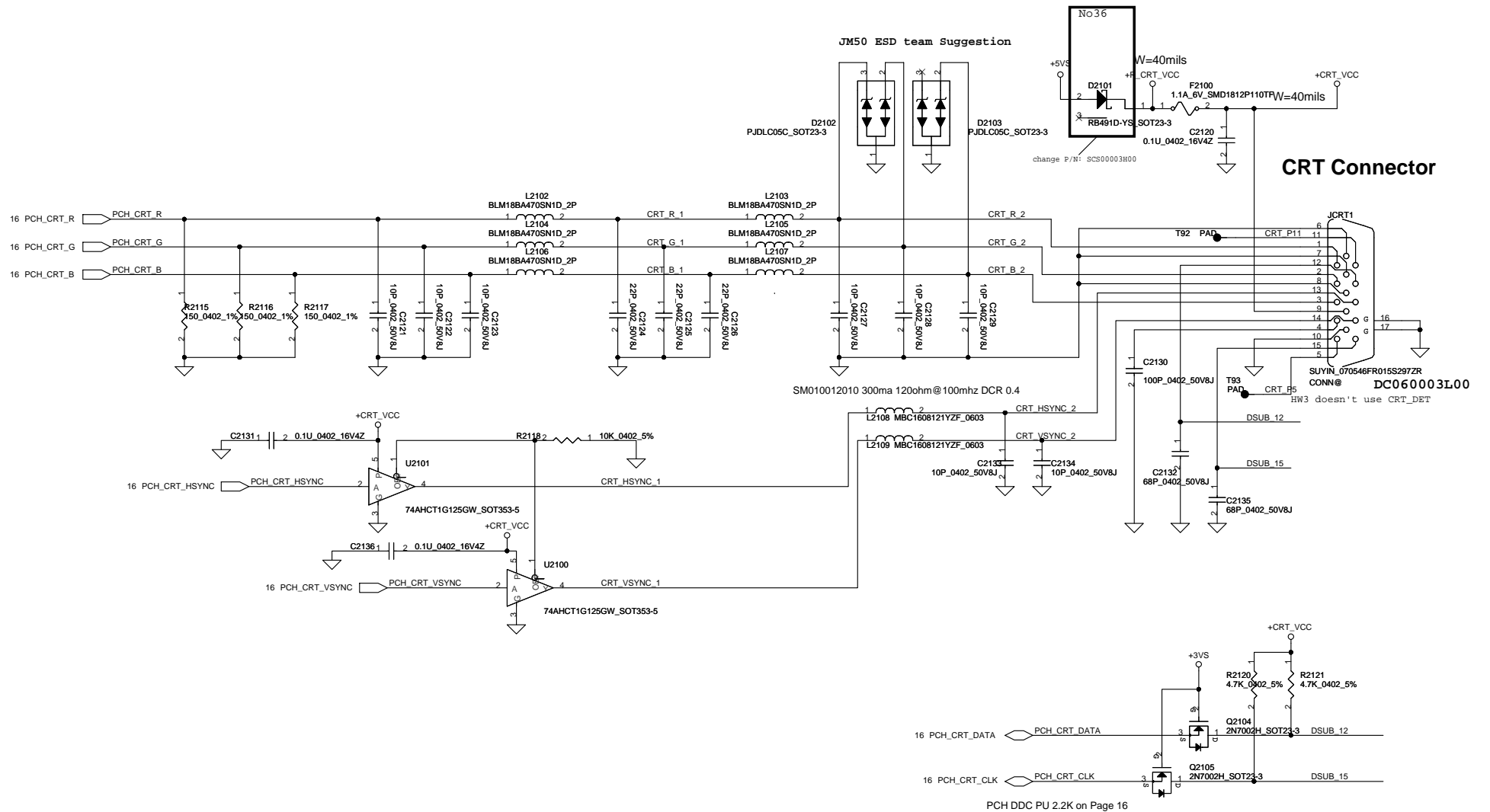
No1  
No44

XCLK_417
0 277MHz (Default)
1 Reserved

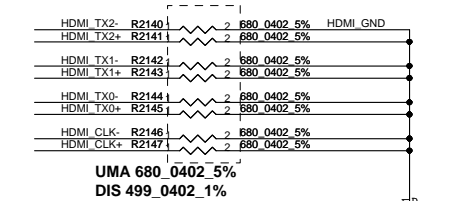
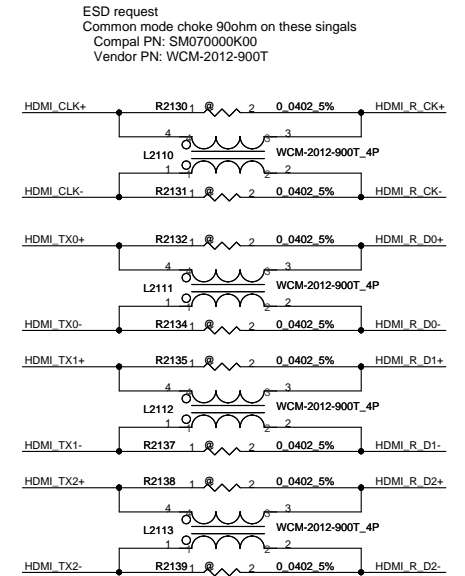
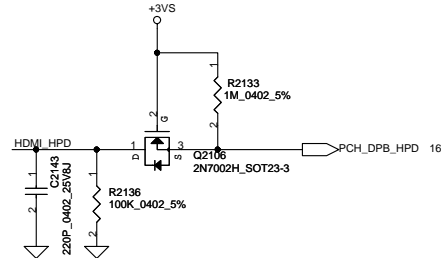
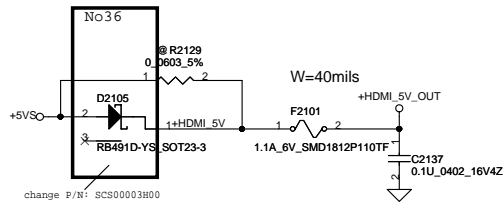
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				Date:	Tuesday, December 14, 2010
				Sheet	33 of 57



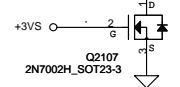
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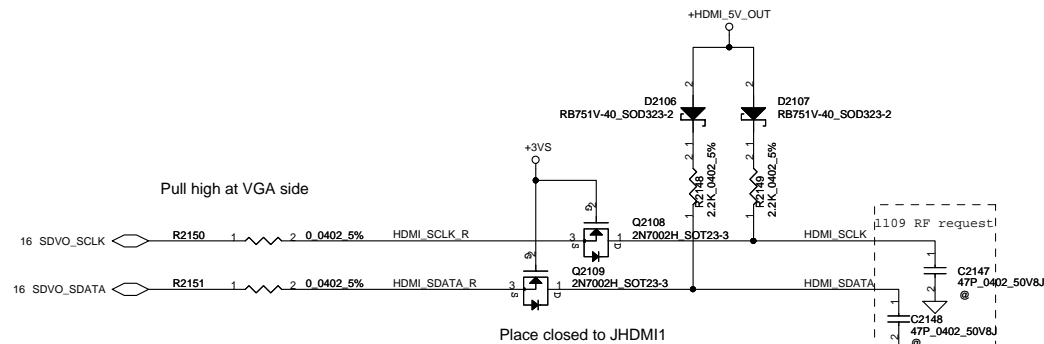
UMA 680\_0402\_5%  
DIS 499\_0402\_1%



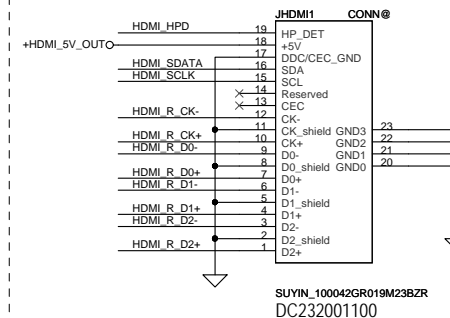
UMA	16	PCH_DP8_N0	C2138	2	1	.1U_0402_16V7K	HDMI_TX2-
	16	PCH_DP8_P0	C2139	2	1	.1U_0402_16V7K	HDMI_TX2+
	16	PCH_DP8_N1	C2140	2	1	.1U_0402_16V7K	HDMI_TX1-
	16	PCH_DP8_P1	C2141	2	1	.1U_0402_16V7K	HDMI_TX1+
	16	PCH_DP8_N2	C2142	2	1	.1U_0402_16V7K	HDMI_TX0-
	16	PCH_DP8_P2	C2144	2	1	.1U_0402_16V7K	HDMI_TX0+
	16	PCH_DP8_N3	C2145	2	1	.1U_0402_16V7K	HDMI_CLK-
	16	PCH_DP8_P3	C2146	2	1	.1U_0402_16V7K	HDMI_CLK+

NVIDA Recommend 05/10

Not reserved



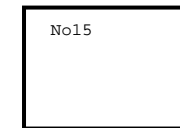
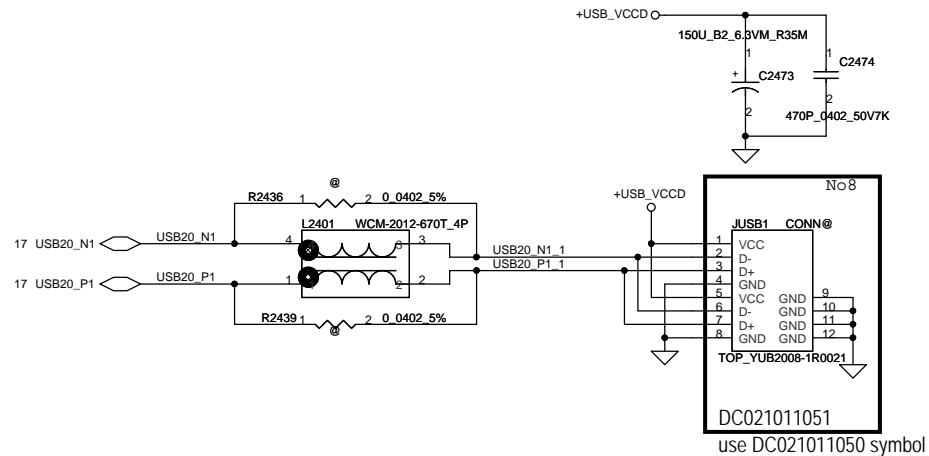
HDMI connector



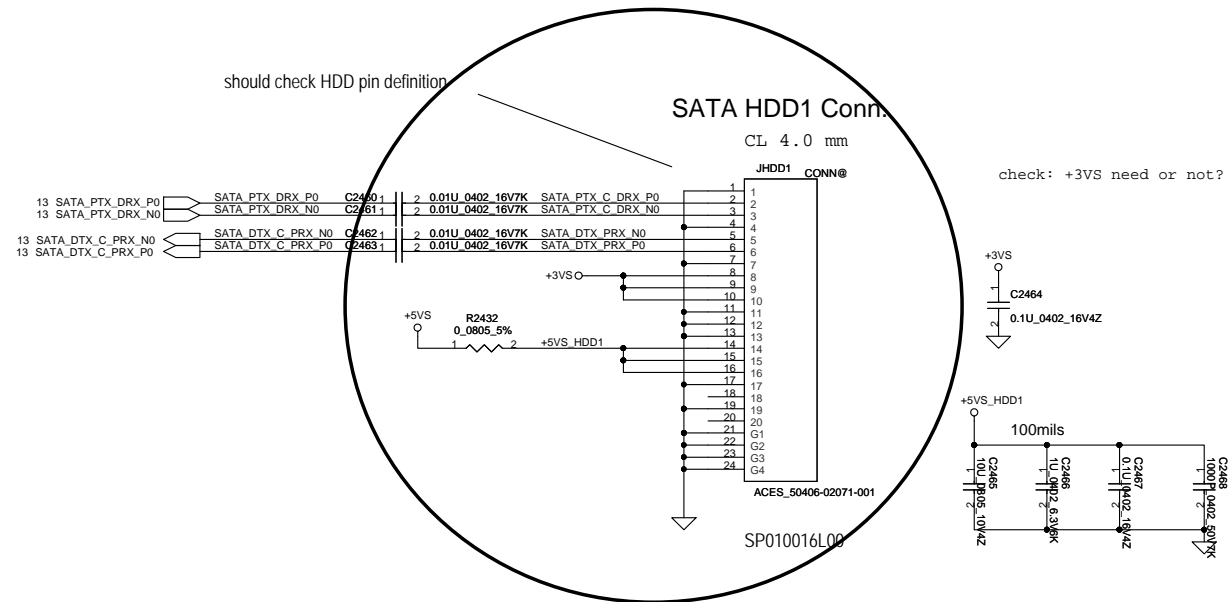
SUYIN\_100042GR019M23B2R  
DC232001100

From layout request, change footprint  
SUYIN\_100042GR019M23B2R\_19P-S

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				Size	Document Number	Rev
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				Date:	Tuesday, December 14, 2010	Sheet 36 of 57

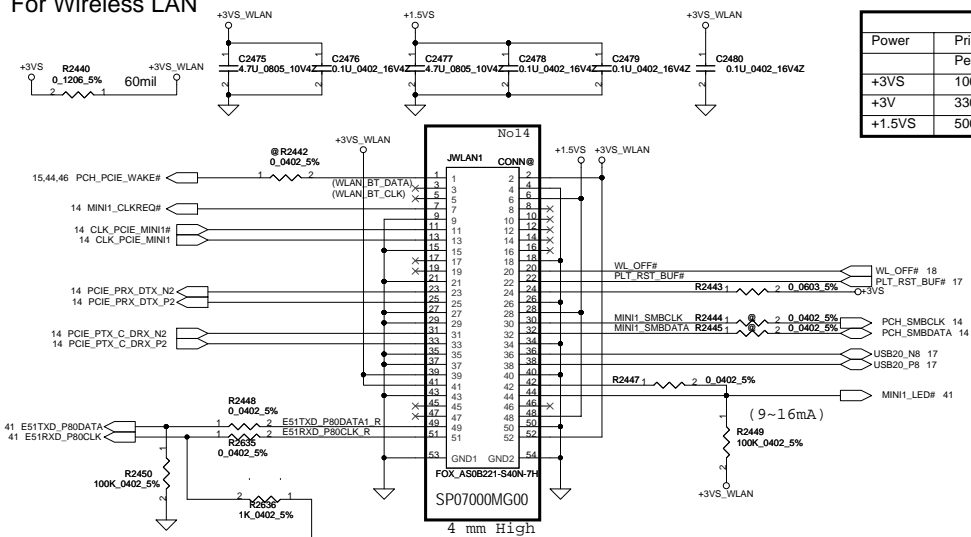


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				Size Document Number Custom 4019BI			
				Rev A			
				Date: Tuesday, December 14, 2010 Sheet 37 of 57			

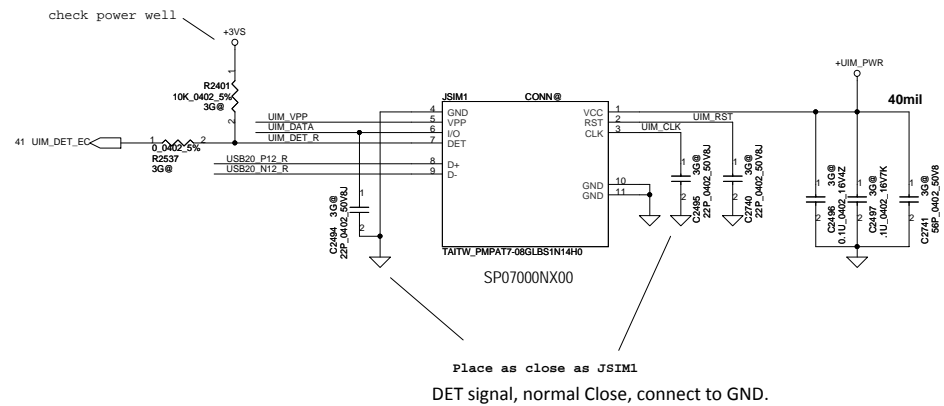
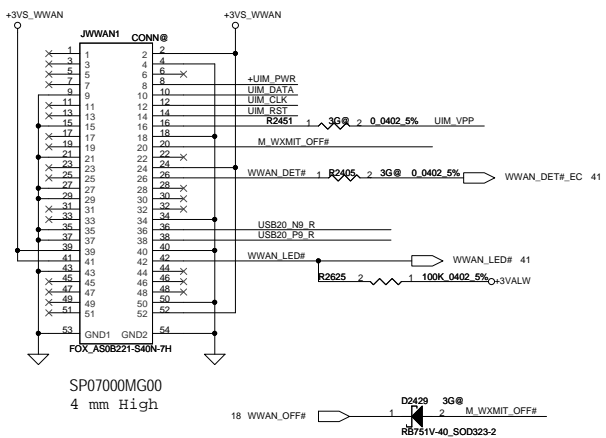
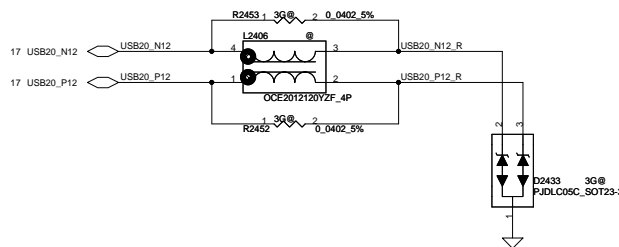
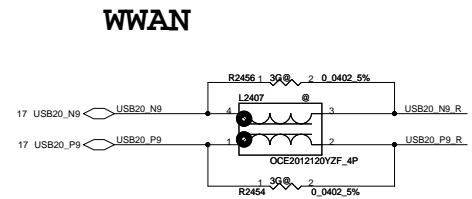
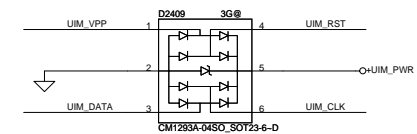
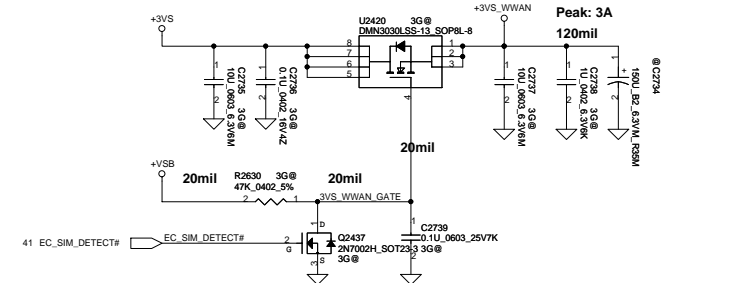
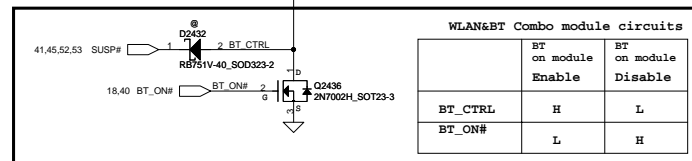


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For Wireless LAN



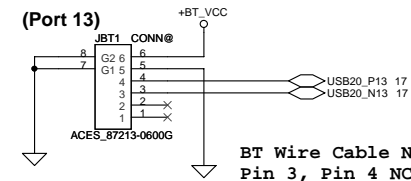
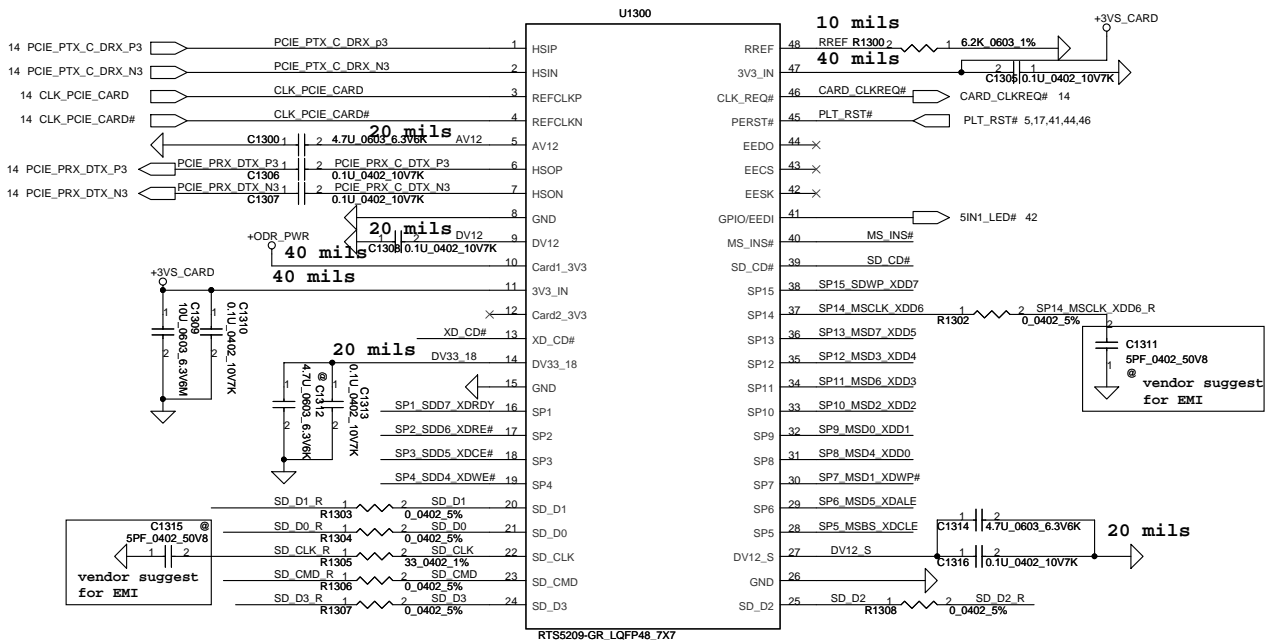
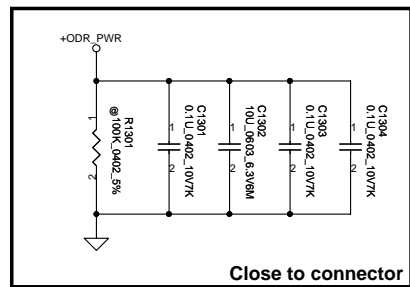
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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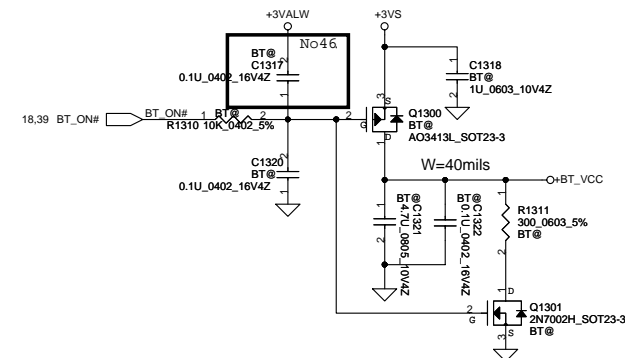
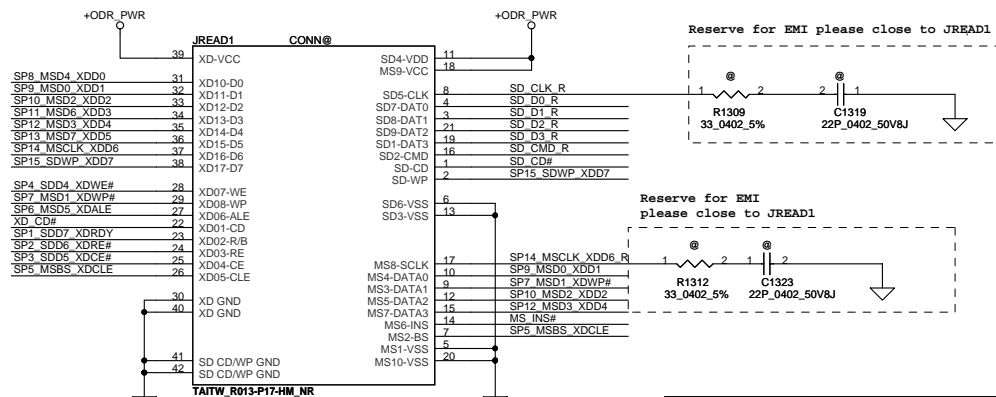
No 41, for measurement

Diagram illustrating a measurement setup (No 41) for a resistor R1313. The circuit is enclosed in a dashed box. It shows a 3V source connected to a resistor R1313 (0.0805\_5%) and a 40 mils gap, which is then connected to a 3V source labeled +3V5\_CARD. The entire circuit is enclosed in a dashed box.



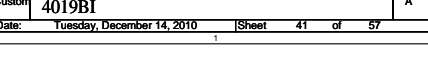
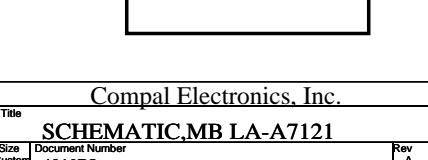
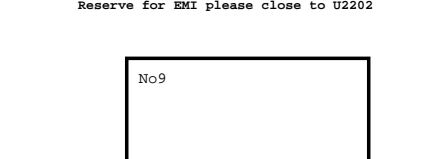
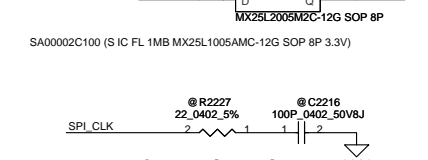
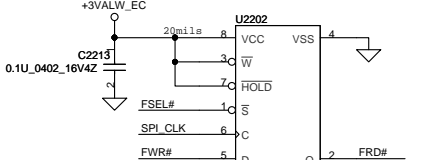
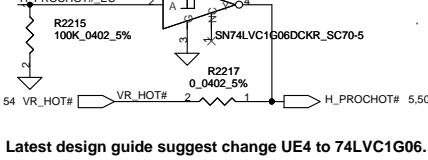
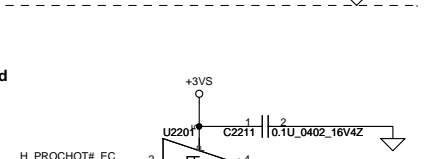
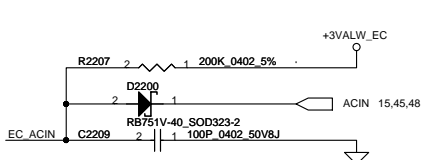
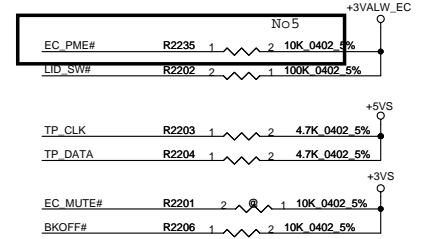
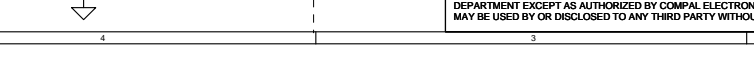
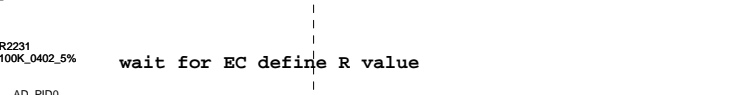
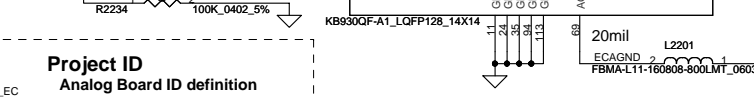
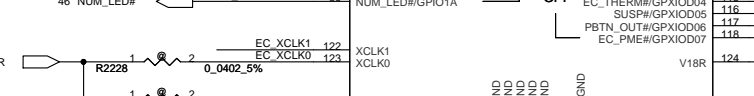
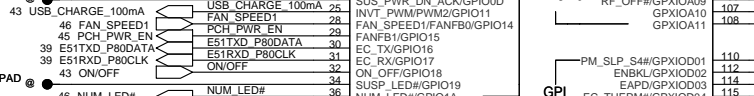
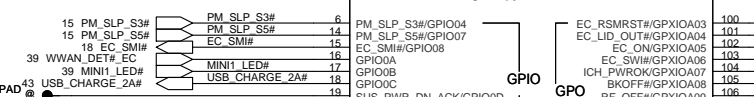
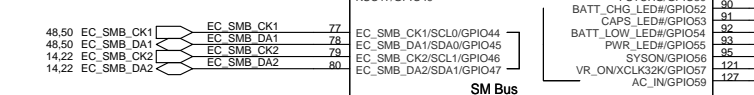
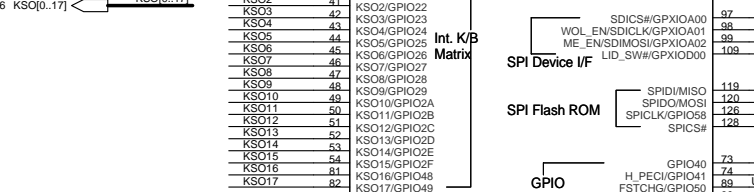
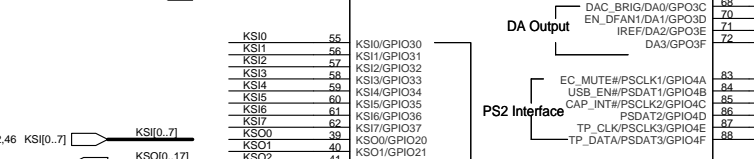
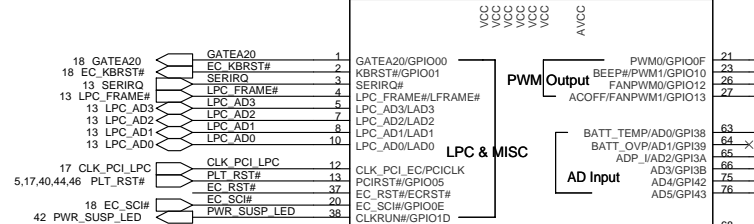
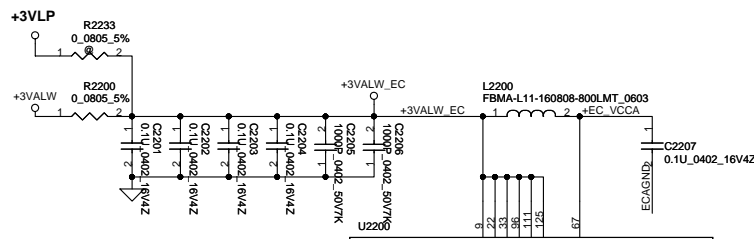
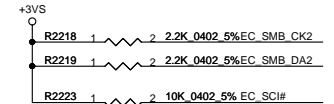
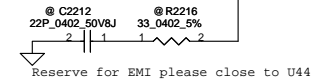
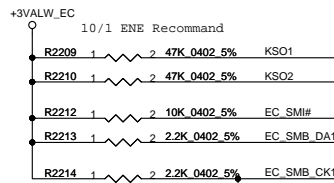
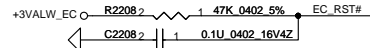
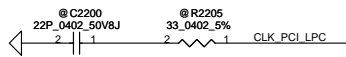
BT Wire Cable Note:  
Pin 3, Pin 4 NC

SP02000FR00



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**Board ID**  
Analog Board ID definition,  
Please see page 3.

**Project ID**  
Analog Board ID definition

wait for EC define R value

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(Left) JKB1 CONN@

Pin	Signal
1	KS00
2	KS01
3	KS02
4	KS03
5	KS04
6	KS05
7	KS06
8	KS07
9	KS08
10	KS09
11	KS010
12	KS011
13	KS012
14	KS013
15	KS014
16	KS015
17	KS016
18	KS017
19	KS10
20	KS11
21	KS12
22	KS13
23	KS14
24	KS15
25	KS16
26	KS17

























G1 27  
G2 28

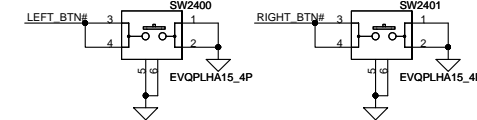
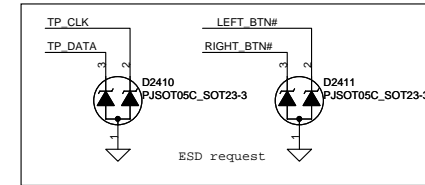
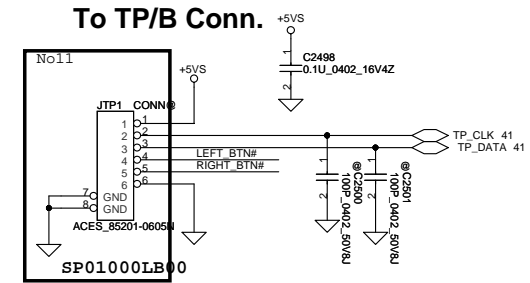
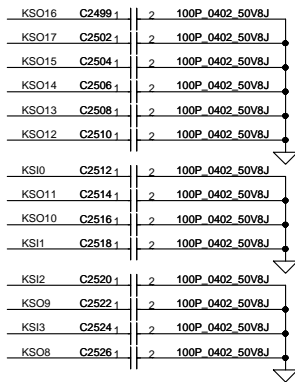
ACES\_85201-26051

KSJ[0..7]  KSJ[0..7] 41.46

KSO[0..17]  KSO[0..17] 41.46

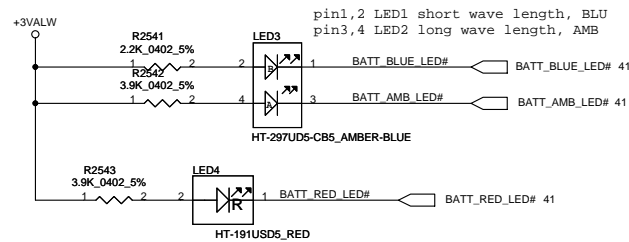
KS	CS	1	2	100P_0402_50V8J
KSO7	C2503			
KSO6	C2505			
KSO5	C2507			
KSO4	C2509			
KSO3	C2511			
KSJ4	C2513			
KSO2	C2515			
KSO1	C2517			
KSO0	C2519			
KSJ5	C2521			
KSJ6	C2523			
KSJ7	C2525			



**LED**

The schematic diagram shows the LED driver circuit for the HT-297UD5-CB5\_AMBER-BLUE LED. The circuit is powered by +3VS. It includes two resistors: R2459 (2.2K\_0402\_5%) and R2460 (3.9K\_0402\_5%). The LED is labeled LED1 and HT-297UD5-CB5\_AMBER-BLUE. The circuit is enclosed in a dashed oval.

Top View LED with Blue/Amber/Red Color



# Reserved

41 PWR\_SUSP\_LED

R2546  
100K\_0402\_5%

2

Q2432A  
2N7002KDWHT\_SOT363-6

PWR\_SUSP\_LED#

41 PWR\_LED

R2547  
100K\_0402\_5%

5

Q2432B  
2N7002KDWHT\_SOT363-6

PWR\_LED#

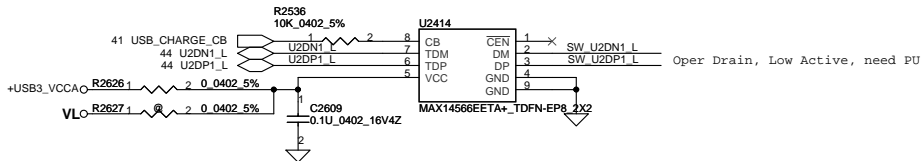
10/2

LED Status	Power/SUS		Battery		3G/WLAN		Bluetooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		

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## USB Host Charger

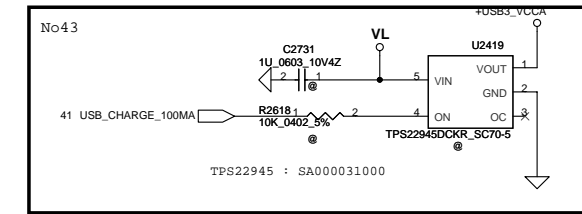
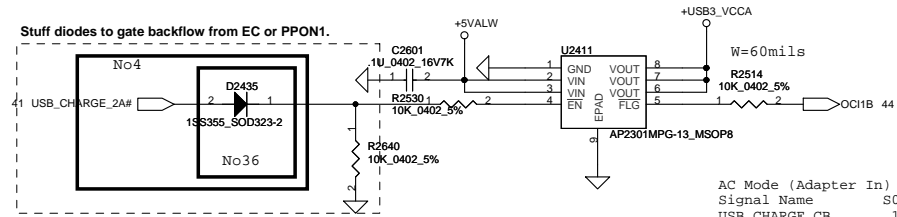


CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM

U37 EN# active at S0, S5(AC) and S5(DC)

S0	S5(AC)	S5(DC)	EN#	ACTIVE	OFF	USB_CHARGE_2A#	PPON1
				ACTIVE	OFF	LOW	LOW
				ACTIVE	OFF	LOW	LOW
				ACTIVE	OFF	LOW	LOW

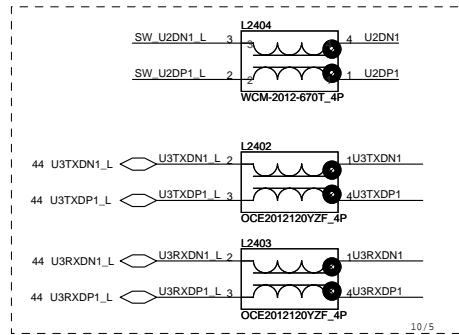
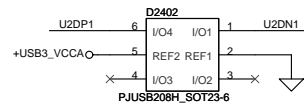
Stuff diodes to gate backflow from EC or PPON1.



AC Mode (Adapter In)  
Signal Name S0 S3 S5  
USB\_CHARGE\_CB 1 0 0  
USB\_CHARGE\_2A# 0 0 0

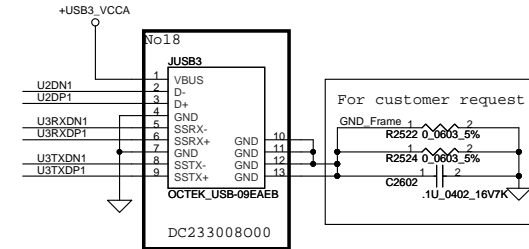
DC Mode (Battery >30%)  
Signal Name S0 S3 S5  
USB\_CHARGE\_CB 1 0 0  
USB\_CHARGE\_2A# 0 0 0

DC Mode (Battery <30%)  
Signal Name S0 S3 S5  
USB\_CHARGE\_CB 1 0 0  
USB\_CHARGE\_2A# 0 1 1

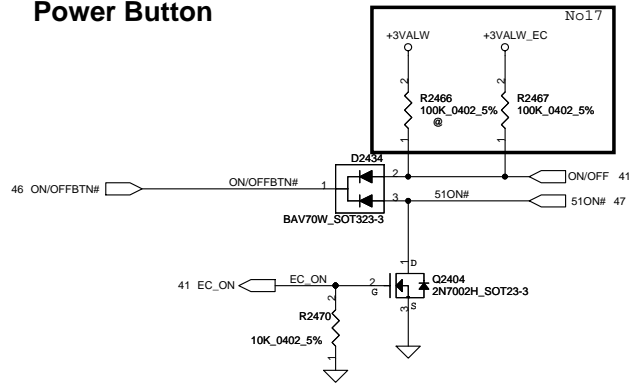


USB\_CHARGE\_CB Switch Control Bit, 0:Auto Detection, 1:Pass-through  
USB\_CHARGE\_2A# Enable 2A USB Power Switch (Low active)

## USB3.0 Connector

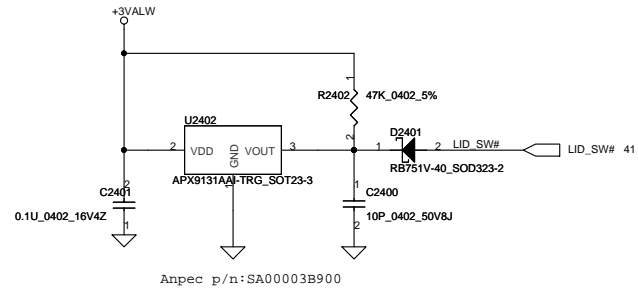


## Power Button

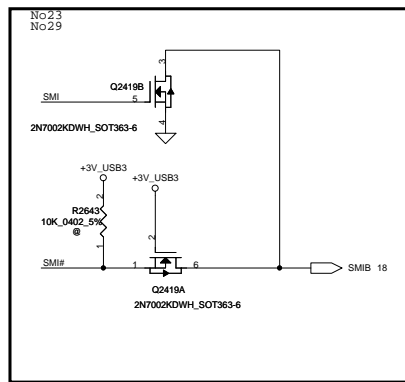
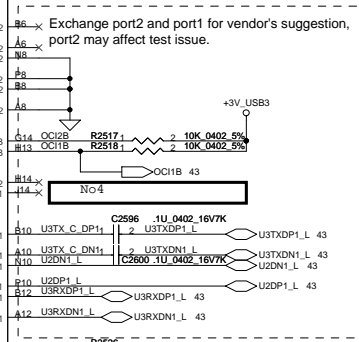
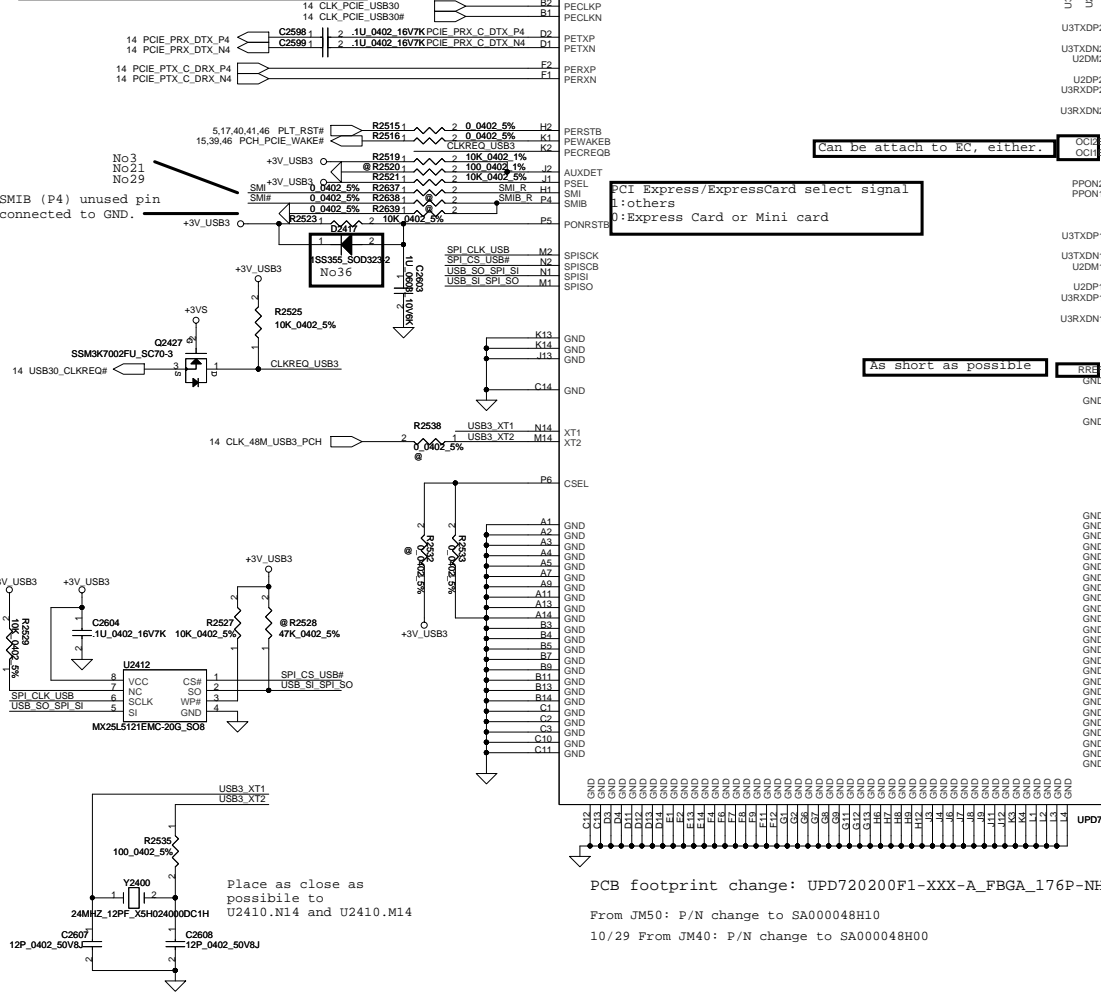
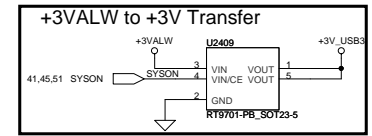
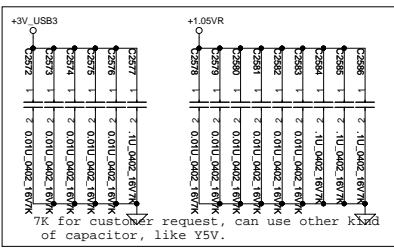
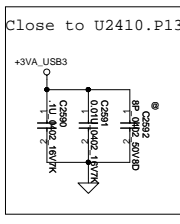
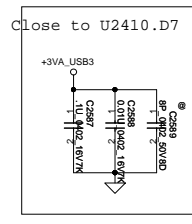
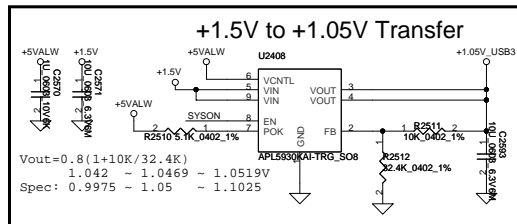


## Lid Switch

(Hall Effect Switch)



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				Custom		4019BI		A	
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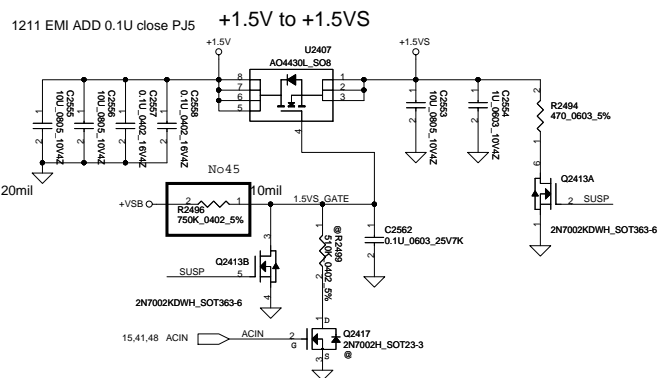
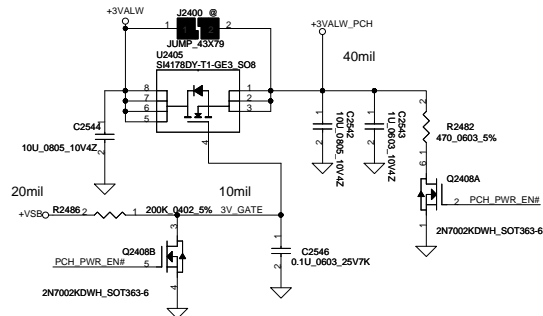
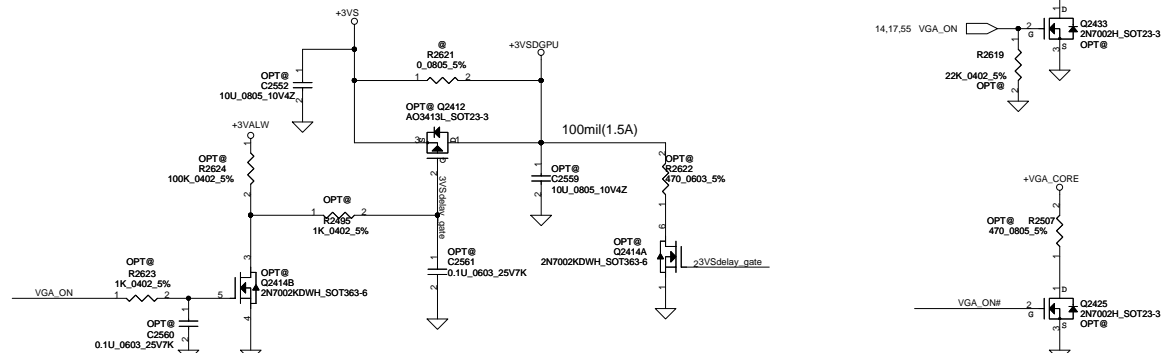


Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41

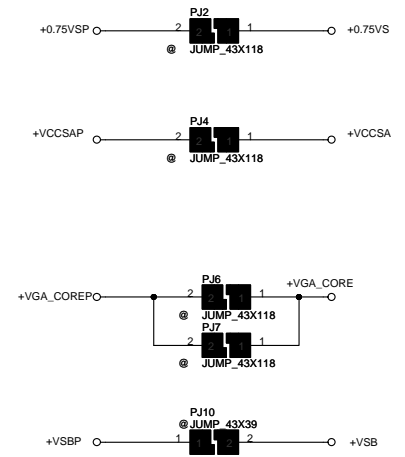
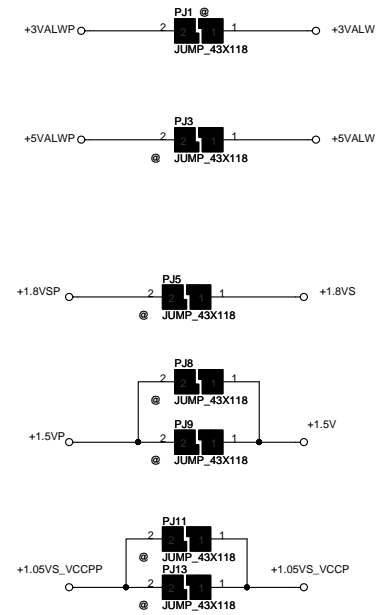
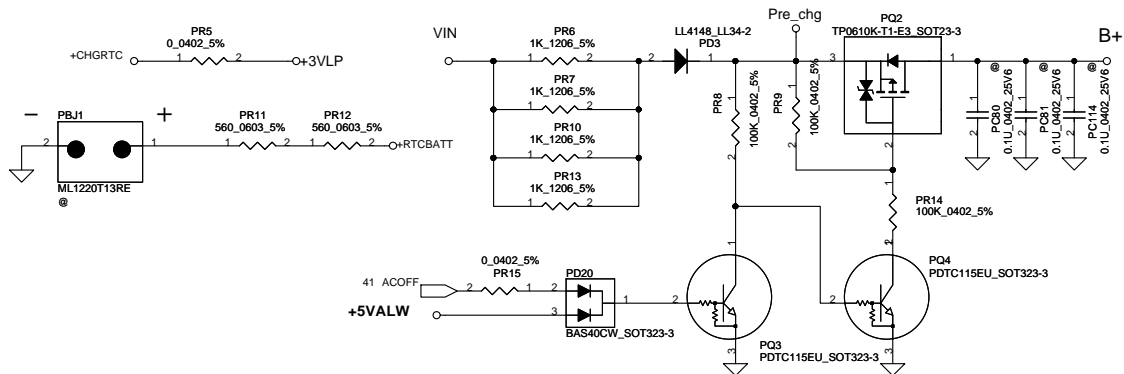
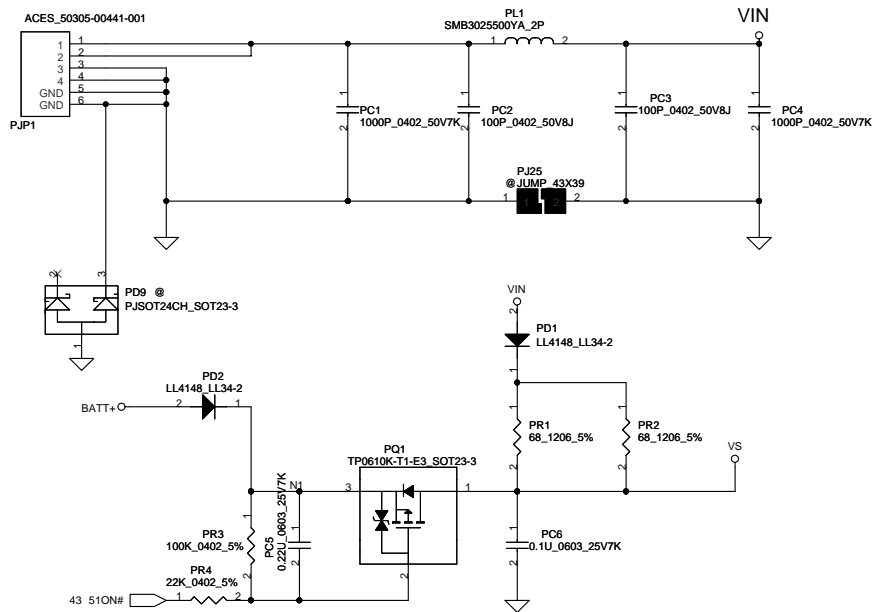
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**MOS needed!**  
+3VALW TO +3VALW(PCH AUX Power)  
Short J5 for PCH VCCSUS3.3

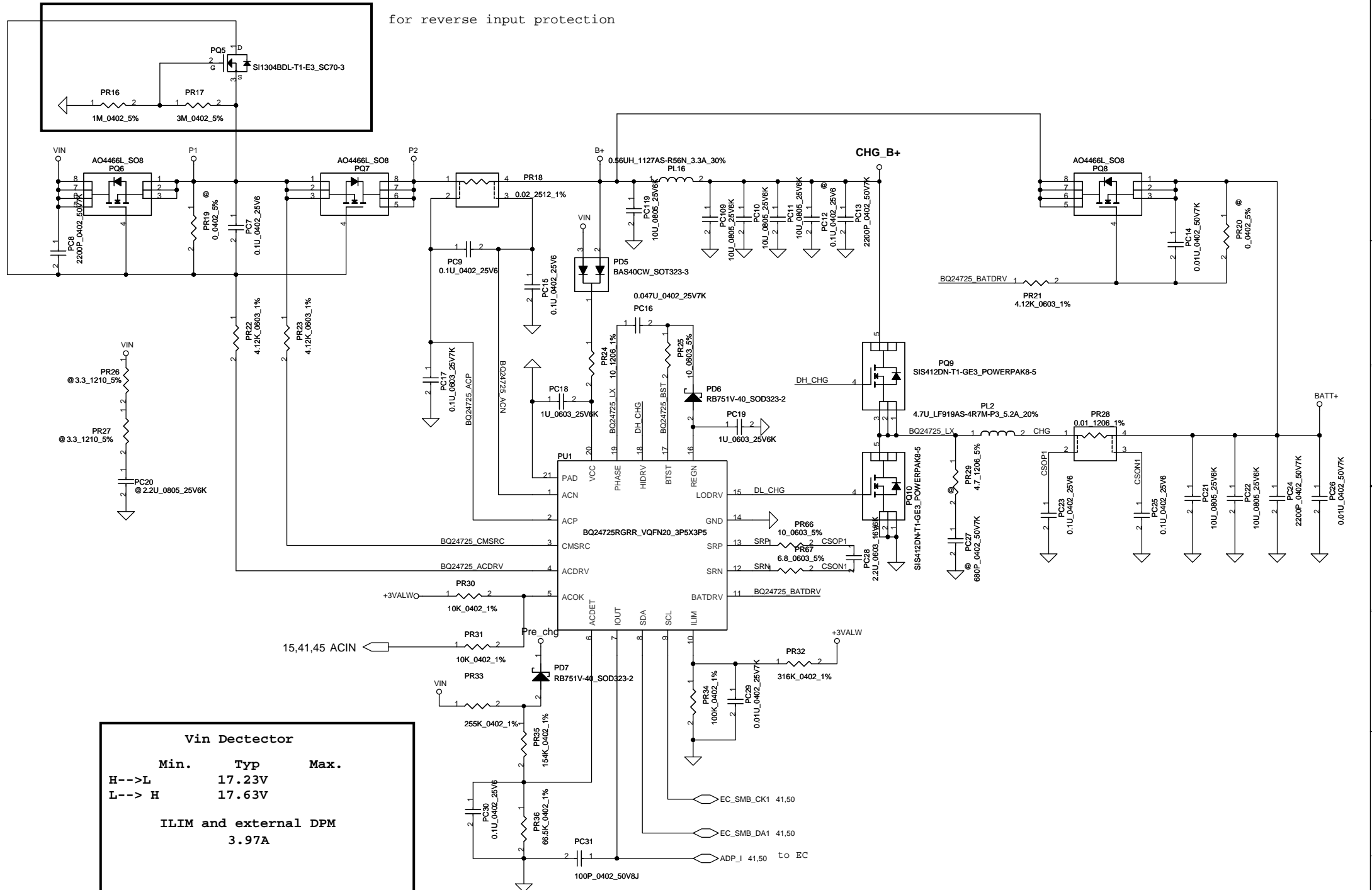
[illegible][illegible]

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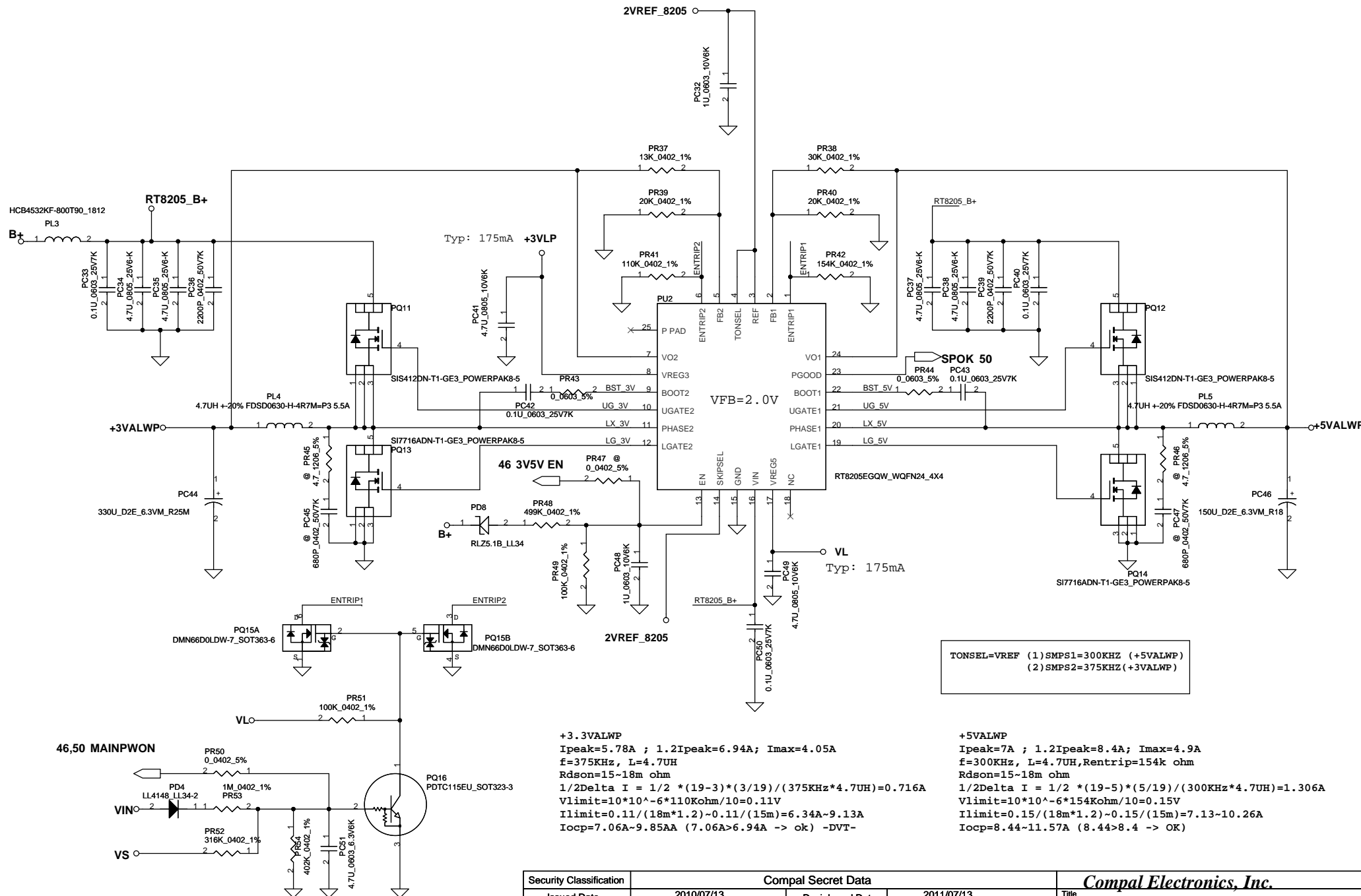


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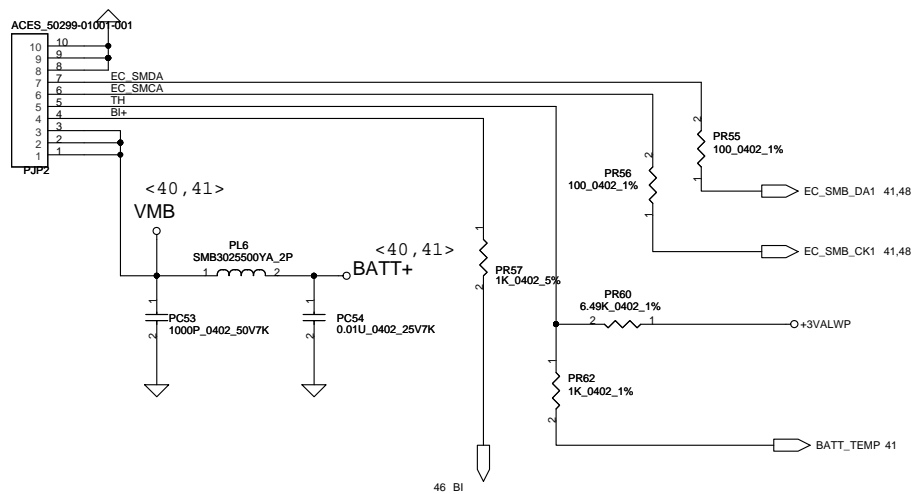




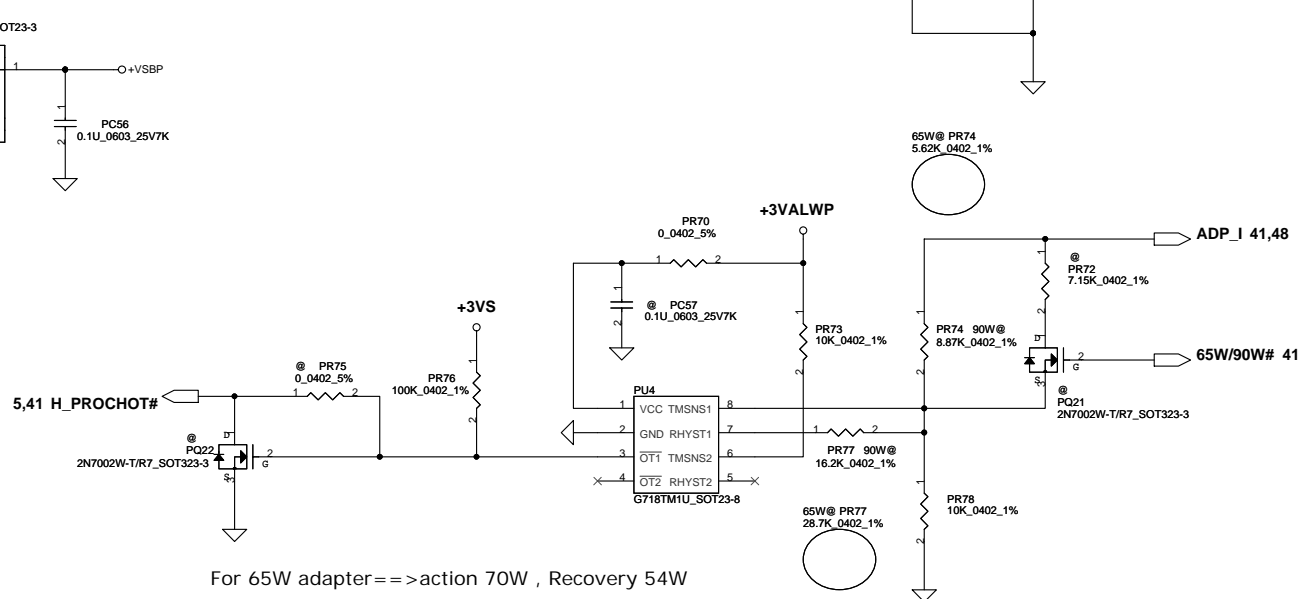
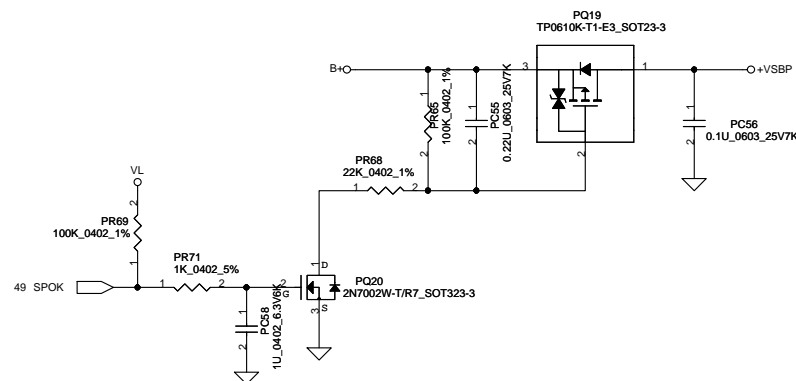
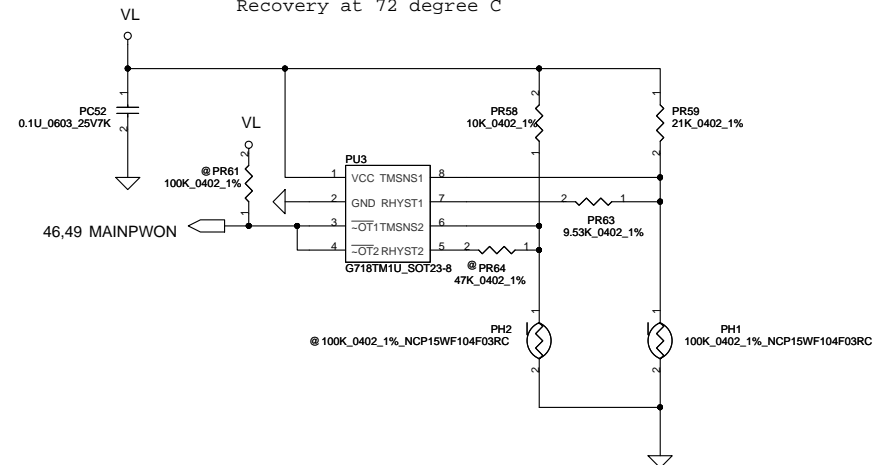
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)  
(2)SMPS2=375KHZ (+3VALWP)

+3.3VALWP  
Ipeak=5.78A ; 1.2Ipeak=6.94A; Imax=4.05A  
f=375KHz, L=4.7UH  
Rdson=15~18m ohm  
1/2Delta I = 1/2 \* (19-3)\*(3/19)/(375KHz\*4.7UH)=0.716A  
Vlimit=10\*10^-6\*110Kohm/10=0.11V  
Ilimit=0.11/(18m\*1.2)~0.11/(15m)=6.34A~9.13A  
Iocp=7.06A~9.85AA (7.06A>6.94A -> ok) -DVT-

+5VALWP  
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A  
f=300KHz, L=4.7UH, Rentrip=154k ohm  
Rdson=15~18m ohm  
1/2Delta I = 1/2 \* (19-5)\*(5/19)/(300KHz\*4.7UH)=1.306A  
Vlimit=10\*10^-6\*154Kohm/10=0.15V  
Ilimit=0.15/(18m\*1.2)~0.15/(15m)=7.13~10.26A  
Iocp=8.44~11.57A (8.44>8.4 -> OK)

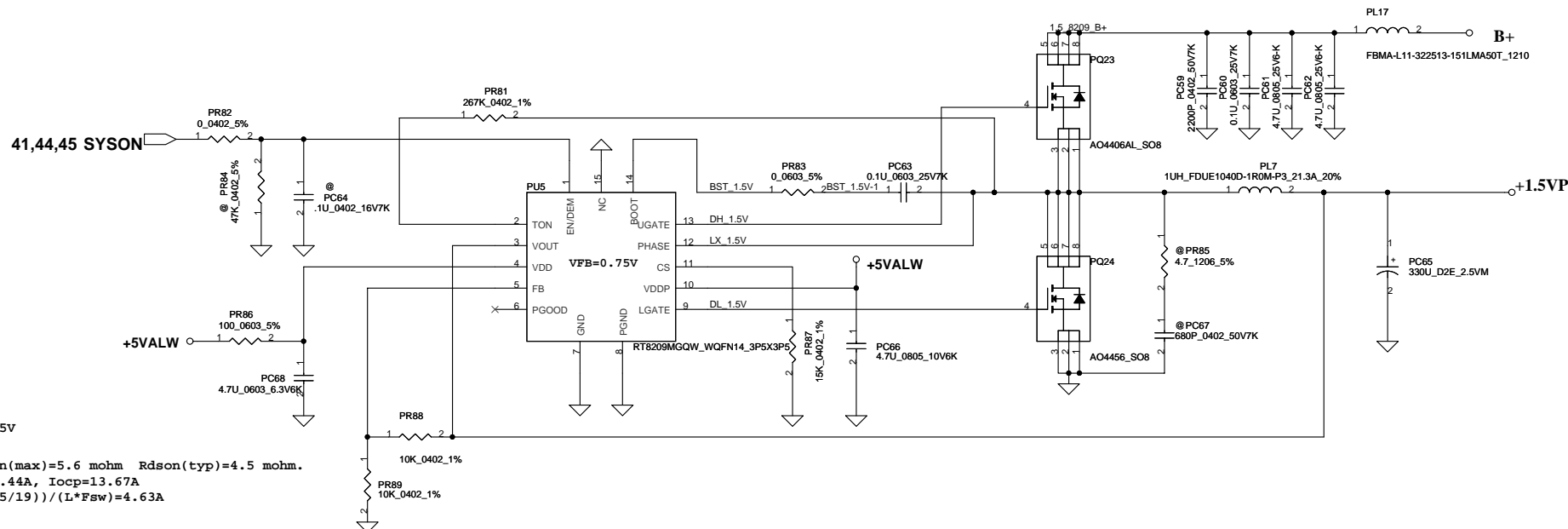


PH1 under CPU botten side :  
CPU thermal protection at 92 degree C  
Recovery at 72 degree C

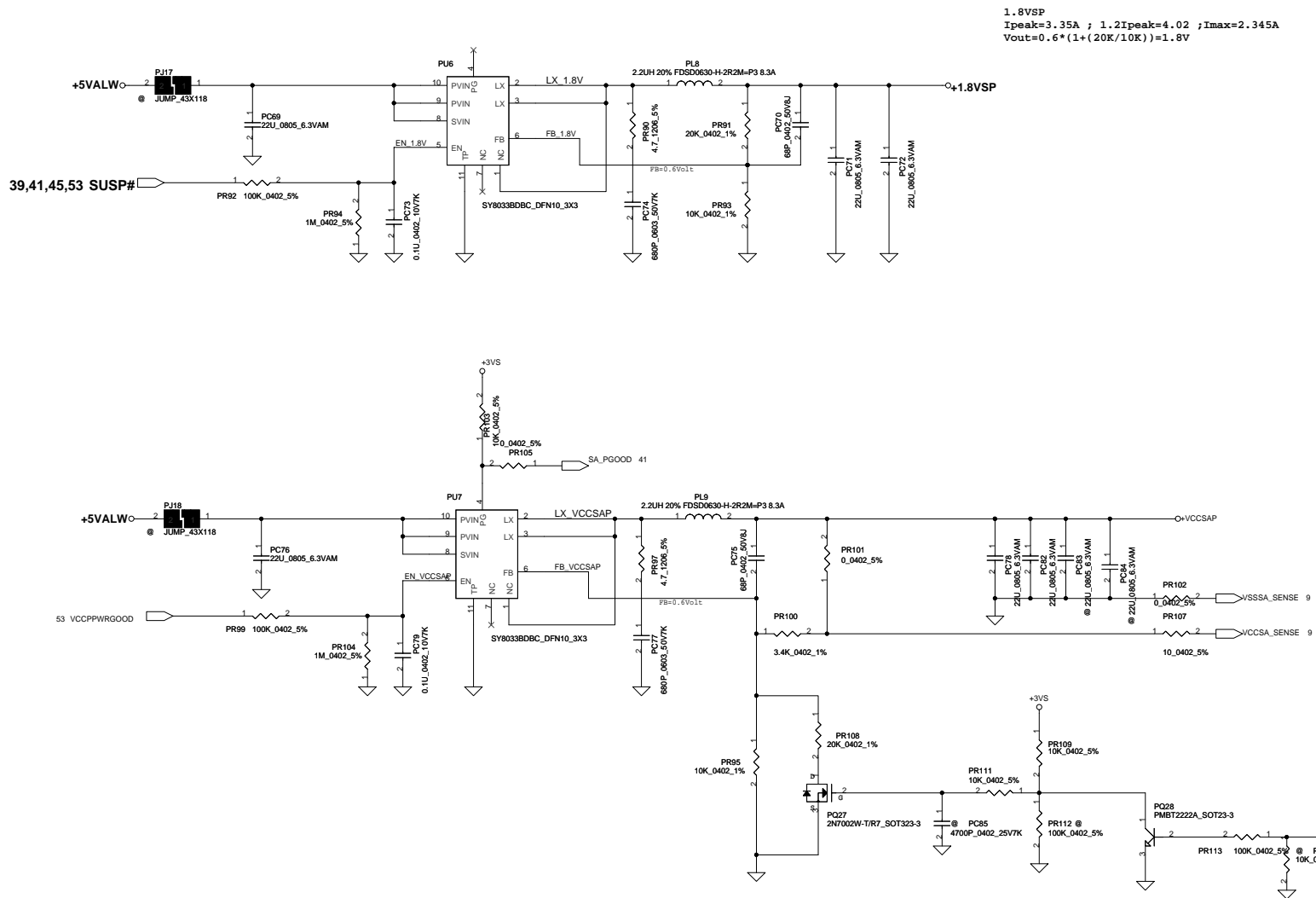


For 65W adapter==>action 70W , Recovery 54W  
For 90W adapter==>action 97W , Recovery 75W

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<Vo=1.5V> VFB=0.75V  
 $V=0.75 \cdot (1+10K/10K)=1.5V$   
 $Fsw=298KHz$   
 $Cout ESR=15m\ ohm\ Rdson(max)=5.6\ mohm\ Rdson(typ)=4.5\ mohm.$   
 $I_{peak}=19.53A, I_{max}=23.44A, I_{ocp}=13.67A$   
 $\Delta I=((19-1.5) \cdot (1.5/19))/(L \cdot Fsw)=4.63A$   
 $\Rightarrow 1/2 \Delta I=2.315A$   
 Choose  $R_{cs}=15K$   
 $I_{ocpmax}=((15K \cdot 11uA)/0.0045)+2.315A=35.65A$   
 $I_{ocpmin}(((15K \cdot 9uA)/(0.0056 \cdot 1.3))+2.315A=23.06A$   
 $I_{ocp}=23.06A-35.65A$



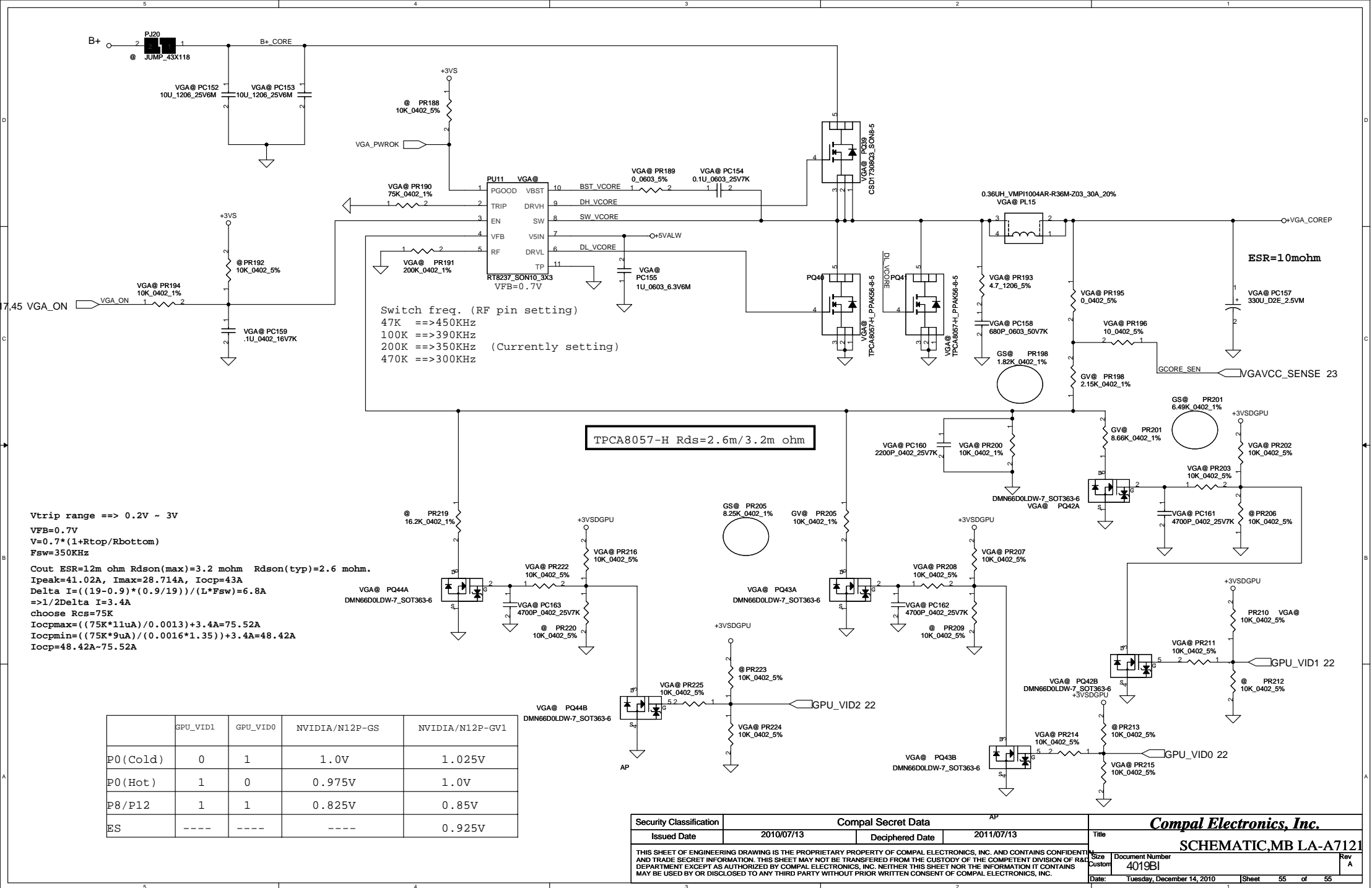
VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA\_SEL to switch High & Low Level for VID[1]  
(ie. VCCSA\_SEL) due to the VID[0] is don't care for this setting.

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11/10 A phase SMT MEMO and Newwork instruction

11/3

No1: P33, change X76e R1491 samsung 64\*16 PD 20K (from 25K)

11/5 SMT MEMO

No1: P44, change YEAM P/N: from SA00003W60 to SA000047Q20, from SA00003VB10 to SA00003Y000

No1: P44, change R2637, R2639, install R2638 for BIOS setting from high active to low active

11/6 rework instruction

No4: P43,44, delete PPGH1 signal and change D2435

11/8 rework instruction

No3: P41, add 10K pull high R2235 for EC\_PME#

11/10 rework instruction

No4: follow NVIDIA Johnson Yeh, for N12P-GV strap pin:  
below strap setting would need to be changed for N12P-GV-S8

1. ROM\_SCLK: pull up 15K ohm.  
2. ROM\_S0: pull up 10K ohm.  
3. STRAP2: pull up 45K ohm.  
4. STRAP3: pull down 5K ohm.  
5. STRAP4: pull down 10K ohm.  
6. STRAP\_REF2, need to stuff with 40K ohm 1%.  
7. PGOOD (pin #7) stuff 10K ohm.

11/11

No1: From DFB request, P46, change SW2402 to SM100001D10 (P51M0 design)

No8: From JM40, change JUSB1 to TopYang DC021011051

11/12

No1: P41, delete cplay EC BIOS ROM U2203

No1: P41, delete JUSB1, add RAPD signal for MUTE function in EC common code

No1: P39, change JUSB1 to JUSB1P, add RAPD signal for MUTE function in EC common code

power circuits JM30\_2010-11-11A-FOR DCIN CONNECTOR.dsn combined

11/15

No12: P46/ P34, change JUSBF1 P/N to SP010000000 (J8 pin), and add DMIC\_CLK, DMIC\_DATA;  
change JUSB1 pin definition, but later should confirm with JM40/50

No13: P46, change JFAM1 P/N to SP02000H900 and swap pin definition

No8: JUSB1 footprint change because not sync up with ME

11/16

No14, P39,, change JWLAM1 pin definition: delete pin 17, 19, 8, 10, 12, 14, 16;  
P17, and delete R249 for no-use PCI CLK to NRAM

No8: change JUSB1 to TopYang DC021011051 and use DC021011050 footprint

No15, P1, delete JUSB1

No16, P43, change C2595 to SGA00002N80

11/19

No19, P43, add ON/OFF pull high R2467 to +3VALM\_EC and unmount R2466

No18, From connector list v28, P43, JUSB3 to DC233008000

No19, P46, (1) delete Open door shut down key (move to sub board), add 1 connector for this function;  
(2) change reset key function, delete unmounted components

No20, P18, For VGA sequence logic, add circuits to DOPU\_PWOK, and from pull high to pull low

11/24

No21, P44, To avoid leakage, delete R2638 0 ohm and add D2418

No22, P46, add R2414 750

11/25

P44, To avoid SMIS leakage, Follow JM40 to do this circuit

No24, P14, reserve SNEUS 0 ohm; R396, R397, R398, R399

11/26

No25, P43, revise USB3.0 function table

power circuits JM30\_20101125.dsn combined

11/29

No26, P18, modify No20, delete VGA\_PWOK path and add PMOS

No27, P46, modify P19, add back unpop parts, and reserve 0 ohm test resistor for open door function, use S18 and S28 to distinguish them

No28, P17, delete VGA\_ON pull high

No29, P44, Modify No23, add pull\_low, change 2M7002

No30, P33, Follow JM40, change R210 to PCN\_RSMRST# instead of PCN\_RSMRST#

No31, P21, Follow JM40, change R1404 for location from R1494.2 to Q1400.1

ROMS: circuits JM30\_20101129.dsn combined

No32, P33, change R210 to 1K

No33, P34, From JM50, for LVDS rise sequence, change R2102 from 1K to 10K, change C2100 from 0.047u to 4.7u

11/30

No34, P18, modify VGA sequence - using 2 NMOS

No35, P46, modify reset and shut down function - delete S18 and S28 optional

12/1

No36, Follow JM40 2nd source,  
D2101, D2105 change to SC800000H000

D2417, D2427, D2435 change to SC100001K00

C186, C1459, C1473, C1474, C1477, C1478, C1484, C1485, C1498, C1506, C1510, C1515, C1538, C1539,  
C1540, C1541, C1566, C1567, C1568, C1569, C1577, C1578, C1579, C1580, C1603, C2466 change to SM000000K80

No37, P34, 46, add RM1 solution for DMIC\_CLK, DMIC\_DATA

power circuits JM30\_20101201.dsn combined

No38, P46, From JM40, modify reset button

No39, P46, From JM40, change D2415 to SM0000007010

No40, From JM40, due to common parts "AND", change U10, U11 to SA000000H00

No41, add +VDS\_CAD0 0 ohm for power consumption measurement

new power circuits JM30\_20101201.dsn combined again

12/3

R542, P46, Follow JM40 add 3V\_LAN MOS to separate 3VALM

date	Func.	No	Page
12/8	ROM change	No43	P33
	description	No44	
	design change	No45	
	ROM change	No46	
12/9	design change	No47	P33